CZC Confidential

CZC Digital technologies Co.,LTD

Board name: Mother Board Schematic

Project name: **CPL S01 (R48)**

Version: VerC

Start Date:JAN 6,2010

VerA Release Data:

1. System Block Diagram & Schematic page description;
2. Power Block Diagram & Discription;
3. Annotations & information;
4. Schematic modify Item and history;
5. Power on & off Sequence;
6. ACPI Mode Switch Timings;
7. Power On Sequence Map;
8. CLOCK Distribution;

Hardware drawing by: _____

Hardware check by: _____

EMI Check by: _____

Power drawing by: _____

Power check by: _____

Manager Sign by: _____

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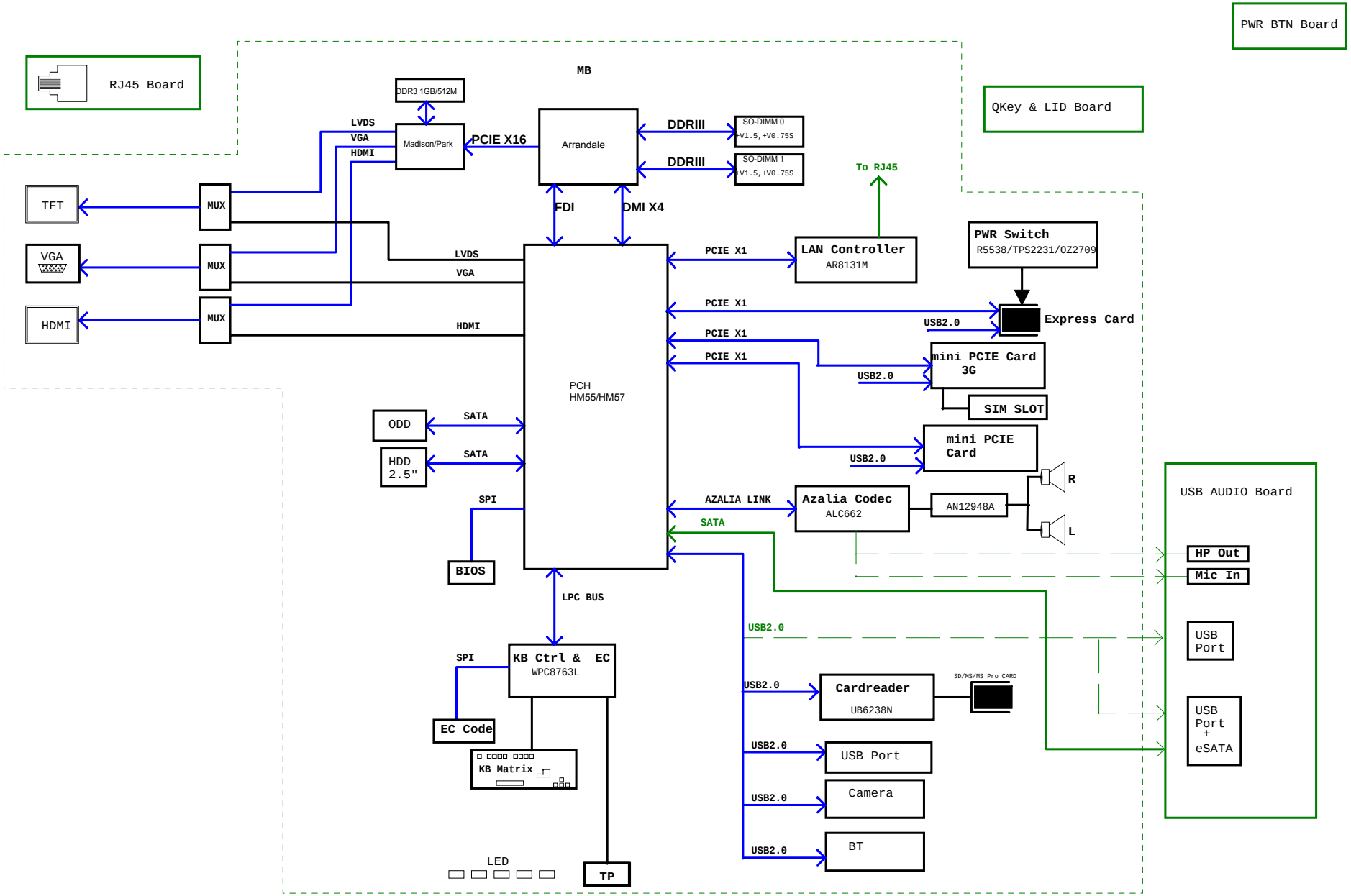
S45 System Block Ver:A



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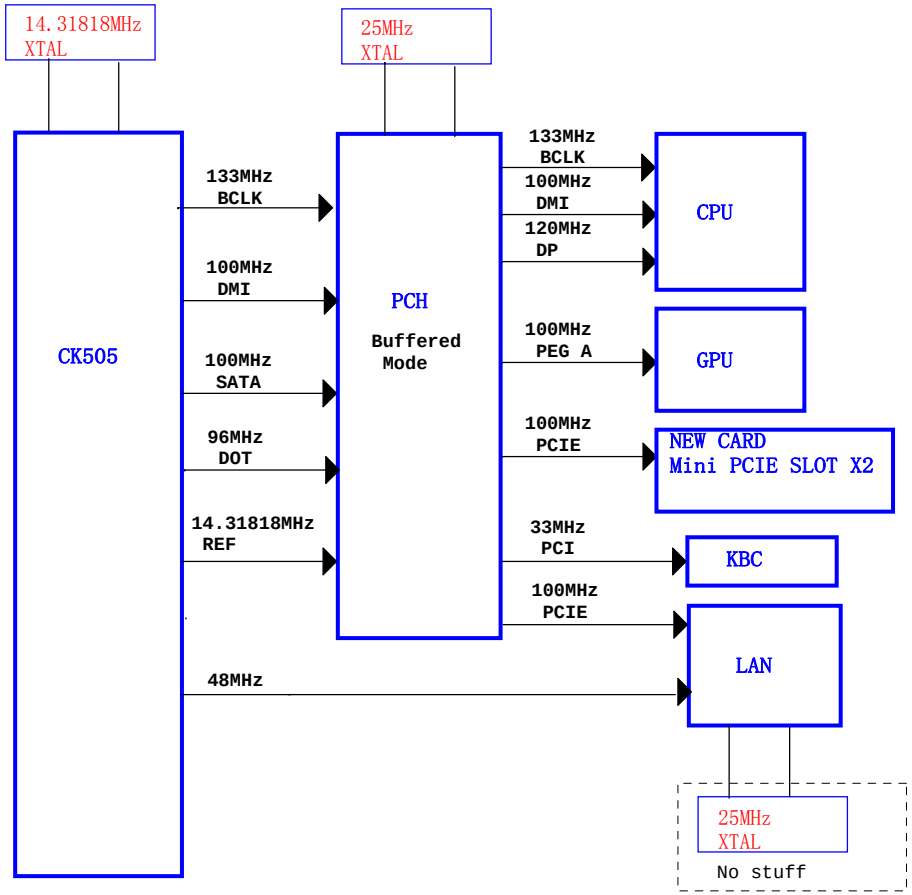
POWER RAIL	AC Mode					Battery Mode				
	S0	S1	S3	S4	S5	S0	S1	S3	S4	S5
+V3.3AUX	ON	ON	ON	ON	ON	ON	ON	ON	OFF	OFF
+V5AUX	ON	ON	ON	ON	ON	ON	ON	ON	OFF	OFF
+V1.5	ON	ON	ON	OFF	OFF	ON	ON	ON	OFF	OFF
+V0.75S	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF
+V5S	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF
+V3.3S	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF
+V1.5S	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF
+V1.8S	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF
+V1.5S	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF
+V1.1S	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF
+Vcore	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF
GFXCORE	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF



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Voltage Rails

+Vcore:0.75V-1.1V

+VDC	Primary DC system power supply(9V-12V)
+VCC_core	Core/VTT voltage for processor
+V1.8S	1.8V For PCH CPU
+V1.1S	1.05V /1.1V For PCH CPU GPU
+V0.75S	0.75V DDRIII Termination voltage
+V1.5S	1.5V for system power
+V1.5	1.5V power rail for DDRIII
+V3.3AUX	3.3V always on power rail
+V3.3S	3.3V main power rail
+V5AUX	5V always on power rail
+V5S	5V main power rail

I2C SMB Address

Device	Address	Hex(W/R)	Bus	Master
Clock Generator	1101 001x	D2H/D3H	SMB_CLK/DATA	PCH
SO-DIMM0	1010 000x	0xA0		
SO-DIMM1	1010 010x	0xA4		
OZ8805LN	0001 011x	16H/17H	EC_I2C_CLK2/DATA2	EC
Thermal Diode G781	1001 100x	98H/99H	EC_I2C_CLK/DATA	

Board stack up description

PCB Layers	
Top(Signal1)	Trace Impedence:50ohm +/-15%
Ground	
Signal2	
Signal3	
Power	
Signal4	
Ground	
Bottom(Signal5)	

PCB Layer Difference signal Impedence list

USB signal difference impedence 85ohm
LVDS signal difference impedence 85ohm
DDRIII signal difference impedence 85ohm
DDRIII CLK signal difference impedence 68ohm

Power States

state \ signal	PM_SLP_S4#	PM_SLP_S3#	+V*AUX	+V*	+V*S	CLOCKS
Full ON		HIGH	ON	ON	ON	ON
S1M(Power On Suspend)		HIGH	ON	ON	ON	LOW
S3(Suspend to RAM)	HIGH	LOW	ON	ON	OFF	OFF
S4(Suspend to DISK)	LOW	LOW	ON	OFF	OFF	OFF
S5/Soft Off With AC IN	LOW	LOW	ON	OFF	OFF	OFF
G3 With Battery	LOW	LOW	OFF	OFF	OFF	OFF

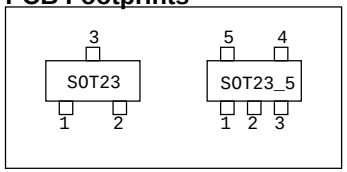
Wake up Events

Wake Events	State Supported(AC)
LID switch from EC	S3 support
Power Button from EC	S3,S4,S5 support
Keyboard from EC	No
USB device	No

[Option]:ns -- Component marked "ns" is not stuff

[Use State]:new --Component Marked "new" is new Materiel.

PCB Footprints



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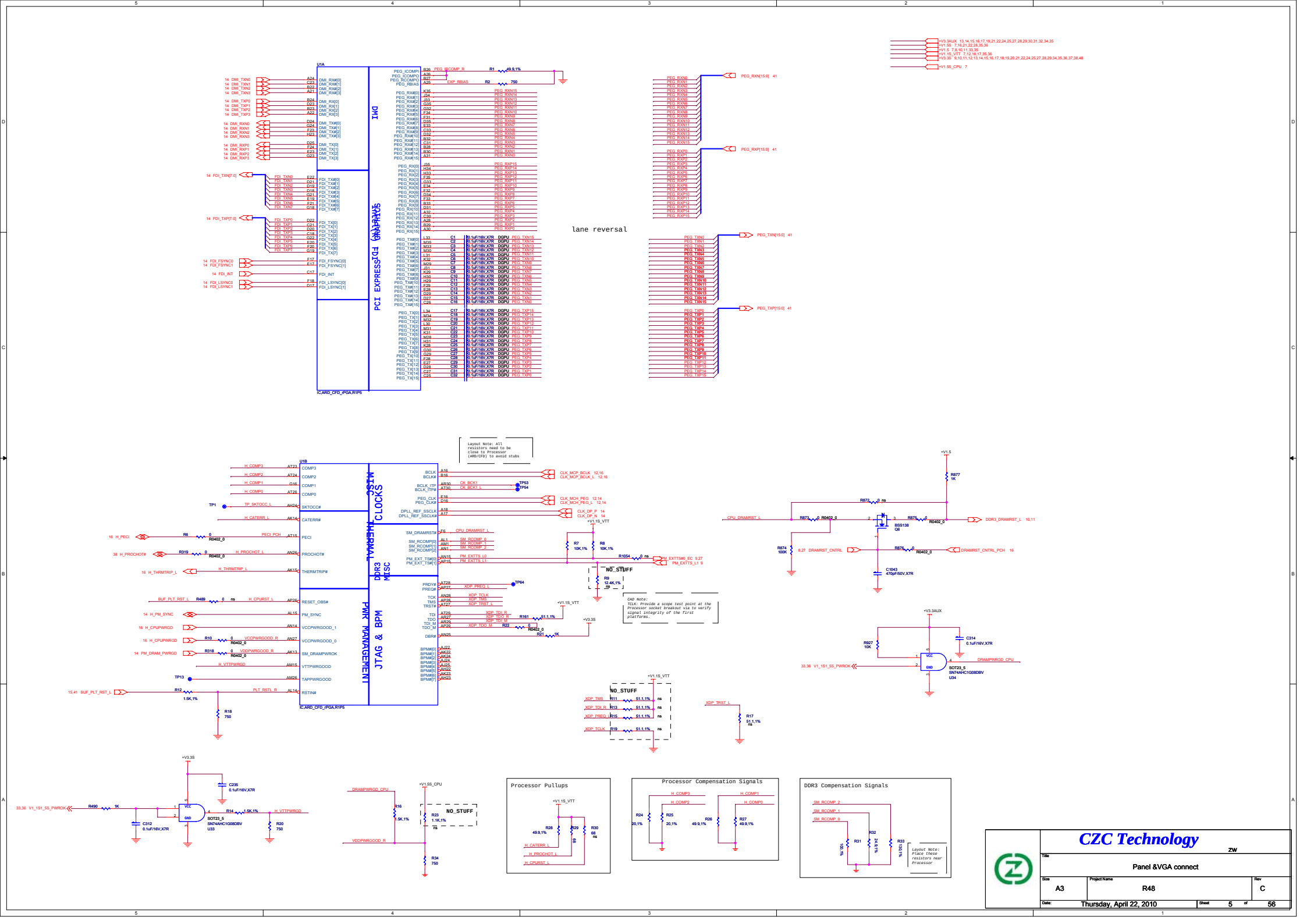

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Title: Panel &VGA connect

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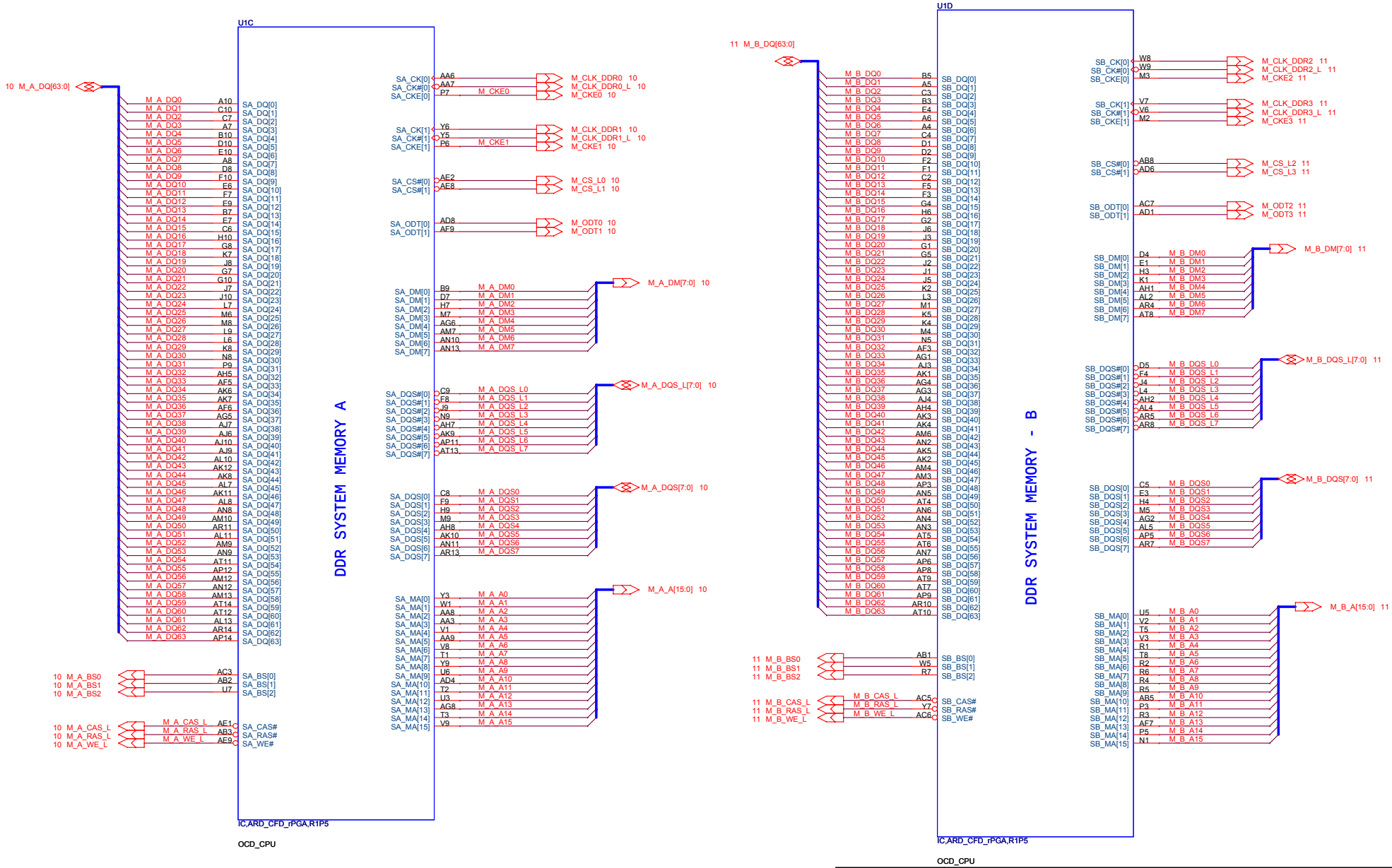

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Title: Panel &VGA connect

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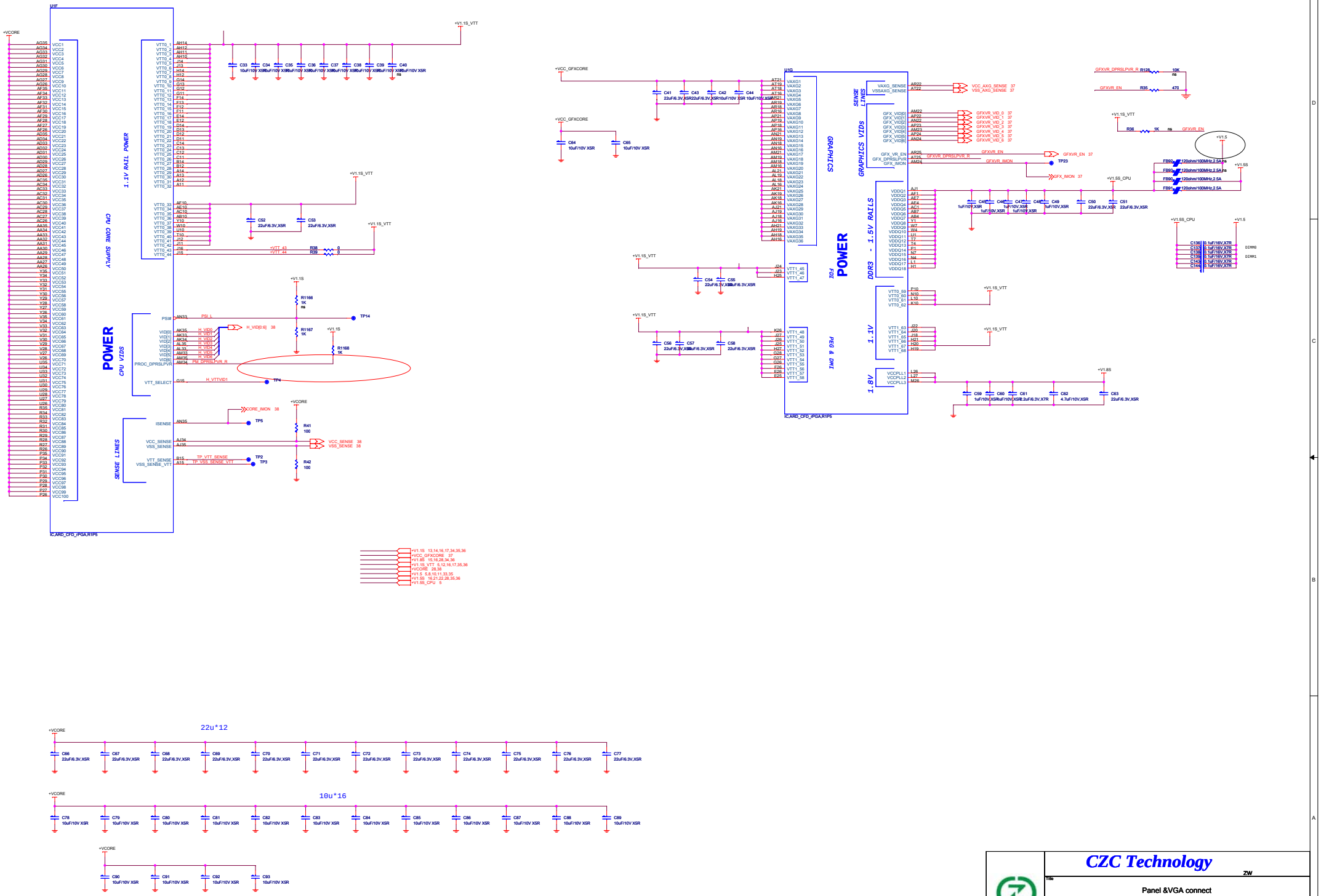

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Title	Panel &VGA connect
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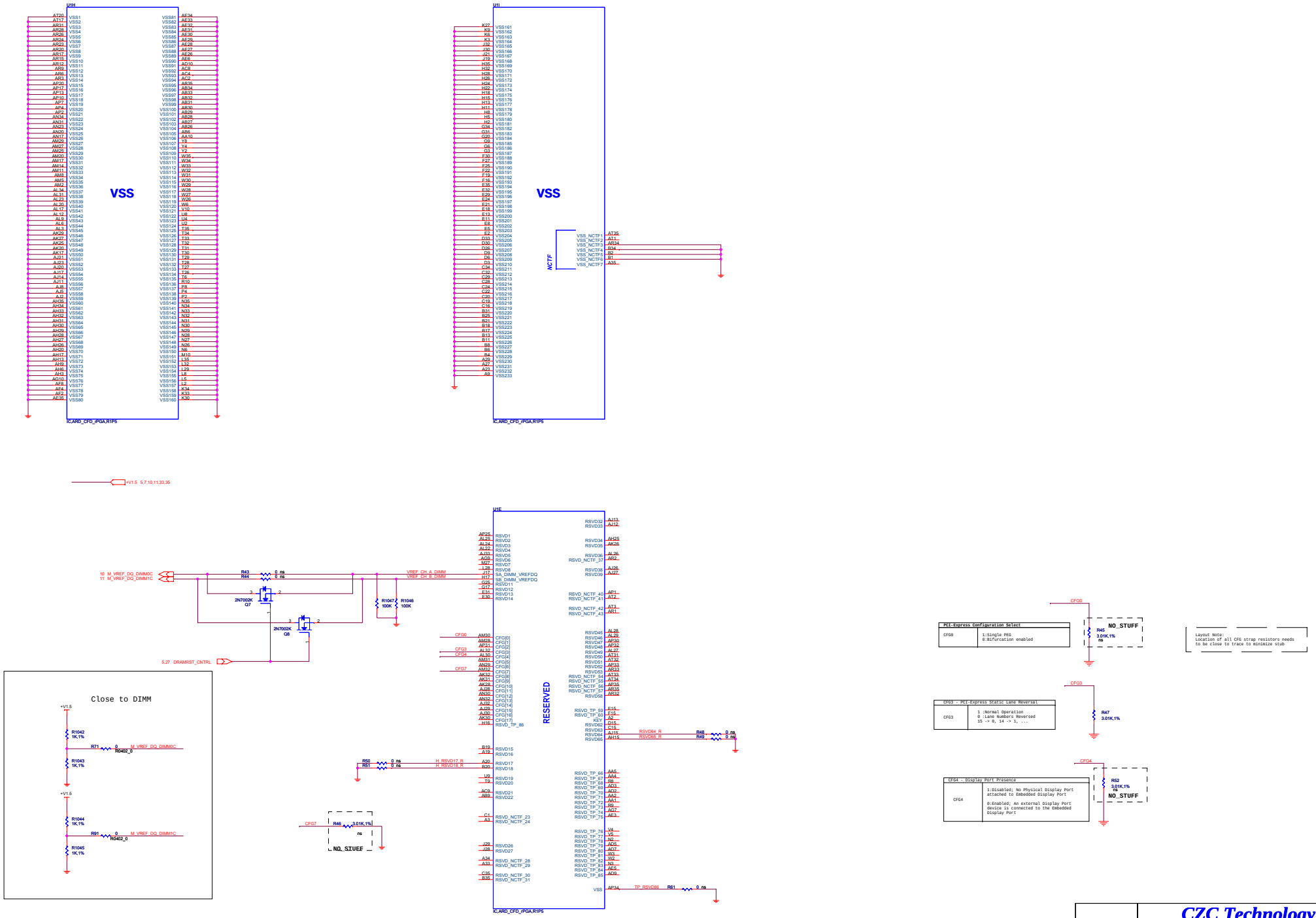

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Title: Panel &VGA connect

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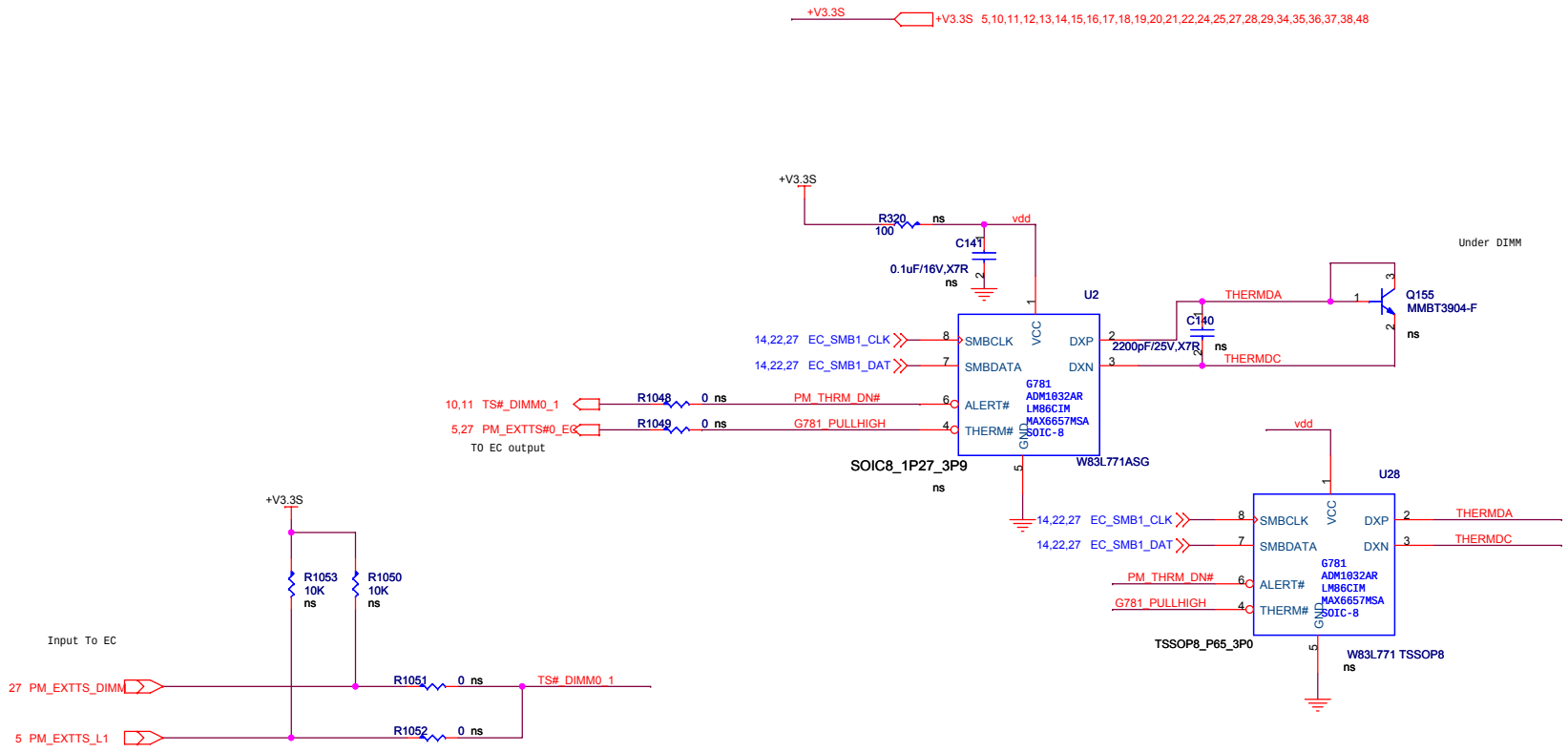

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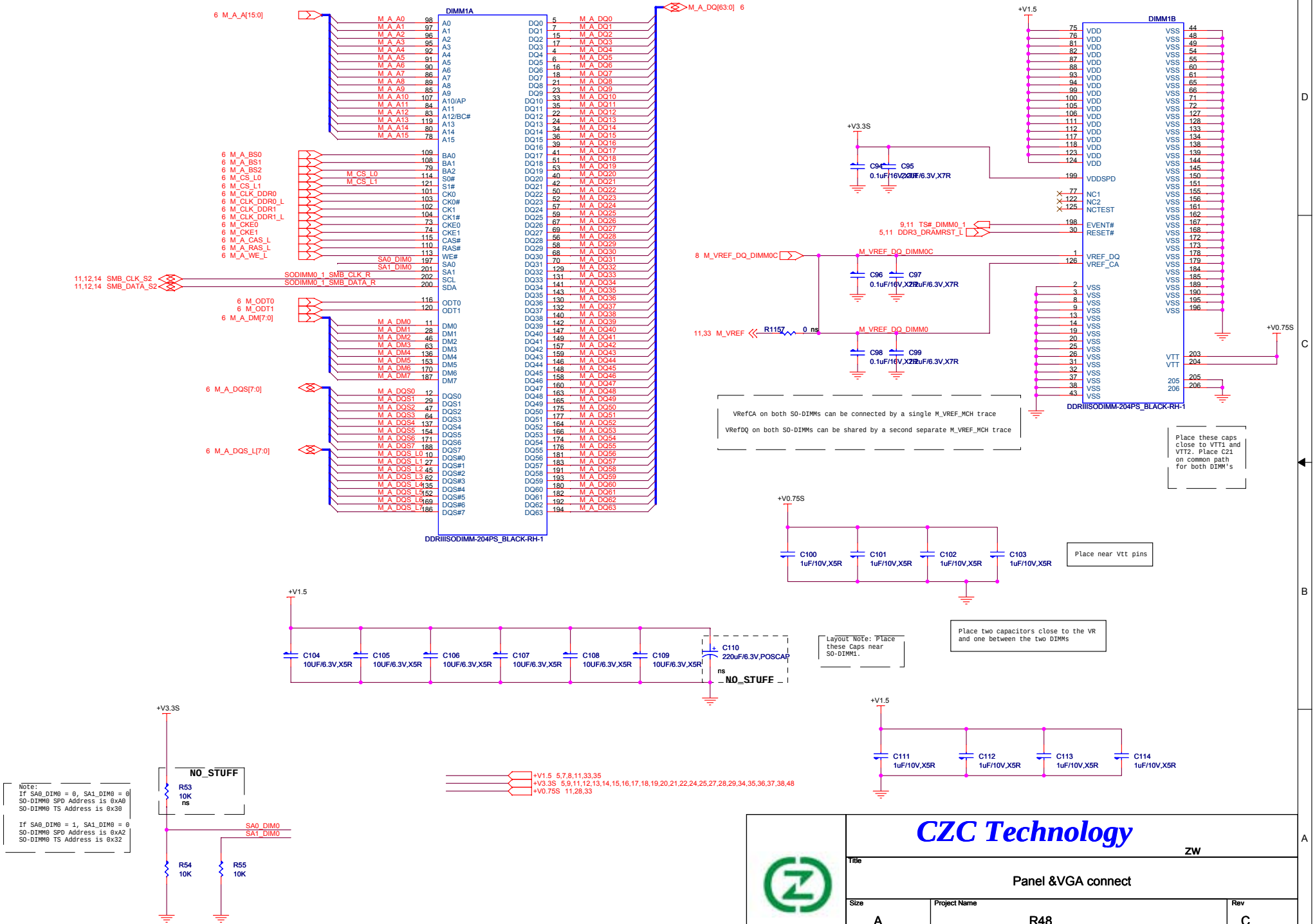
Channel A High :9.2mm



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Channel B High :5.2mm

+V1.5 5,7,8,10,33,35
+V3.3S 5,9,10,12,13,14,15,16,17,18,19,20,21,22,24,25,27,28,29,34,35,36,37,38,48
+V0.75S 10,28,33

DIMM2A — DDRIIISODIMM-204PS_BLACK-RH

6 M_B_A[15:0]: M_B_A0 (98), M_B_A1 (97), M_B_A2 (96), M_B_A3 (95), M_B_A4 (92), M_B_A5 (91), M_B_A6 (90), M_B_A7 (86), M_B_A8 (89), M_B_A9 (85), M_B_A10 (107), M_B_A11 (84), M_B_A12 (83), M_B_A13 (119), M_B_A14 (80), M_B_A15 (78)

6 M_B_BS0 (109), 6 M_B_BS1 (108), 6 M_B_BS2 (79), 6 M_CS_L2 (114), 6 M_CS_L3 (121), 6 M_CLK_DDR2 (101), 6 M_CLK_DDR2_L (103), 6 M_CLK_DDR3 (102), 6 M_CLK_DDR3_L (104), 6 M_CKE2 (73), 6 M_CKE3 (74), 6 M_B_CAS_L (115), 6 M_B_RAS_L (110), 6 M_B_WE_L (113)

SA0_DIM1 (197), SA1_DIM1 (201)

10,12,14 SMB_CLK_S2 (202), 10,12,14 SMB_DATA_S2 (200)

6 M_ODT2 (116), 6 M_ODT3 (120)

6 M_B_DM[7:0]: M_B_DM0 (11), M_B_DM1 (28), M_B_DM2 (46), M_B_DM3 (63), M_B_DM4 (136), M_B_DM5 (153), M_B_DM6 (170), M_B_DM7 (187)

6 M_B_DQS[7:0]: M_B_DQS0 (12), M_B_DQS1 (29), M_B_DQS2 (47), M_B_DQS3 (64), M_B_DQS4 (137), M_B_DQS5 (154), M_B_DQS6 (171), M_B_DQS7 (188)

6 M_B_DQS_L[7:0]: M_B_DQS_L0 (10), M_B_DQS_L1 (27), M_B_DQS_L2 (45), M_B_DQS_L3 (62), M_B_DQS_L4 (135), M_B_DQS_L5 (152), M_B_DQS_L6 (169), M_B_DQS_L7 (186)

M_B_DQ[63:0] 6: M_B_DQ0 (5), M_B_DQ1 (7), M_B_DQ2 (15), M_B_DQ3 (17), M_B_DQ4 (4), M_B_DQ5 (6), M_B_DQ6 (16), M_B_DQ7 (18), M_B_DQ8 (21), M_B_DQ9 (23), M_B_DQ10 (33), M_B_DQ11 (35), M_B_DQ12 (22), M_B_DQ13 (24), M_B_DQ14 (34), M_B_DQ15 (36), M_B_DQ16 (39), M_B_DQ17 (41), M_B_DQ18 (51), M_B_DQ19 (53), M_B_DQ20 (40), M_B_DQ21 (42), M_B_DQ22 (50), M_B_DQ23 (52), M_B_DQ24 (57), M_B_DQ25 (59), M_B_DQ26 (67), M_B_DQ27 (69), M_B_DQ28 (56), M_B_DQ29 (58), M_B_DQ30 (68), M_B_DQ31 (70), M_B_DQ32 (129), M_B_DQ33 (131), M_B_DQ34 (141), M_B_DQ35 (143), M_B_DQ36 (130), M_B_DQ37 (132), M_B_DQ38 (140), M_B_DQ39 (142), M_B_DQ40 (147), M_B_DQ41 (149), M_B_DQ42 (157), M_B_DQ43 (159), M_B_DQ44 (146), M_B_DQ45 (148), M_B_DQ46 (158), M_B_DQ47 (160), M_B_DQ48 (163), M_B_DQ49 (165), M_B_DQ50 (175), M_B_DQ51 (177), M_B_DQ52 (164), M_B_DQ53 (166), M_B_DQ54 (174), M_B_DQ55 (176), M_B_DQ56 (181), M_B_DQ57 (183), M_B_DQ58 (191), M_B_DQ59 (193), M_B_DQ60 (180), M_B_DQ61 (182), M_B_DQ62 (192), M_B_DQ63 (194)

Note:
SO-DIMM1 SPD Address is 0xA4
SO-DIMM1 TS Address is 0x34

SO-DIMM1 is placed farther from the Processor than SO-DIMM0

DIMM2B — DDRIIISODIMM-204PS_BLACK-RH

+V1.5: VDD (75, 76, 81, 82, 87, 88, 93, 94, 99, 100, 105, 106, 111, 112, 117, 118, 123, 124)
VDDSPD (199)
NC1 (77), NC2 (122), NCTEST (125)
9,10 TS#_DIMM0_1 (198), 5,10 DDR3_DRAMRST_L (30) — EVENT#, RESET#
8 M_VREF_DQ_DIMM1C (1) — VREF_DQ, VREF_CA (126)
VSS (2, 3, 8, 9, 13, 14, 19, 20, 25, 26, 31, 32, 37, 38, 43)
VTT (203, 204) → +V0.75S
VSS (205, 206)

+V3.3S: C115 0.1uF/16V,X7R; C116 2.2uF/6.3V,X7R

M_VREF_DQ_DIMM1C: C117 0.1uF/16V,X7R; C118 2.2uF/6.3V,X7R

10,33 M_VREF — R1158 0 ns — M_VREF_DQ_DIMM1: C119 0.1uF/16V,X7R; C120 2.2uF/6.3V,X7R

VRefCA on both SO-DIMMs can be connected by a single M_VREF_MCH trace
VRefDQ on both SO-DIMMs can be shared by a second separate M_VREF_MCH trace

+V0.75S: C121 1uF/10V,X5R; C122 1uF/10V,X5R; C123 1uF/10V,X5R; C124 1uF/10V,X5R

Place near Vtt pins

+V1.5: C125 10uF/10V X5R; C126 10uF/10V X5R; C127 10uF/10V X5R; C128 10uF/10V X5R; C129 10uF/10V X5R; C130 10uF/10V X5R; C131 220uF/2.5V ns

Layout Note: Place these Caps near SO-DIMM1.

+V3.3S: R56 10K — SA1_DIM1; SA0_DIM1 — R57 10K

+V1.5: C132 1uF/10V,X5R; C133 0.1uF/16V,X7R; C134 0.1uF/16V,X7R; C135 0.1uF/16V,X7R

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Title: Panel &VGA connect

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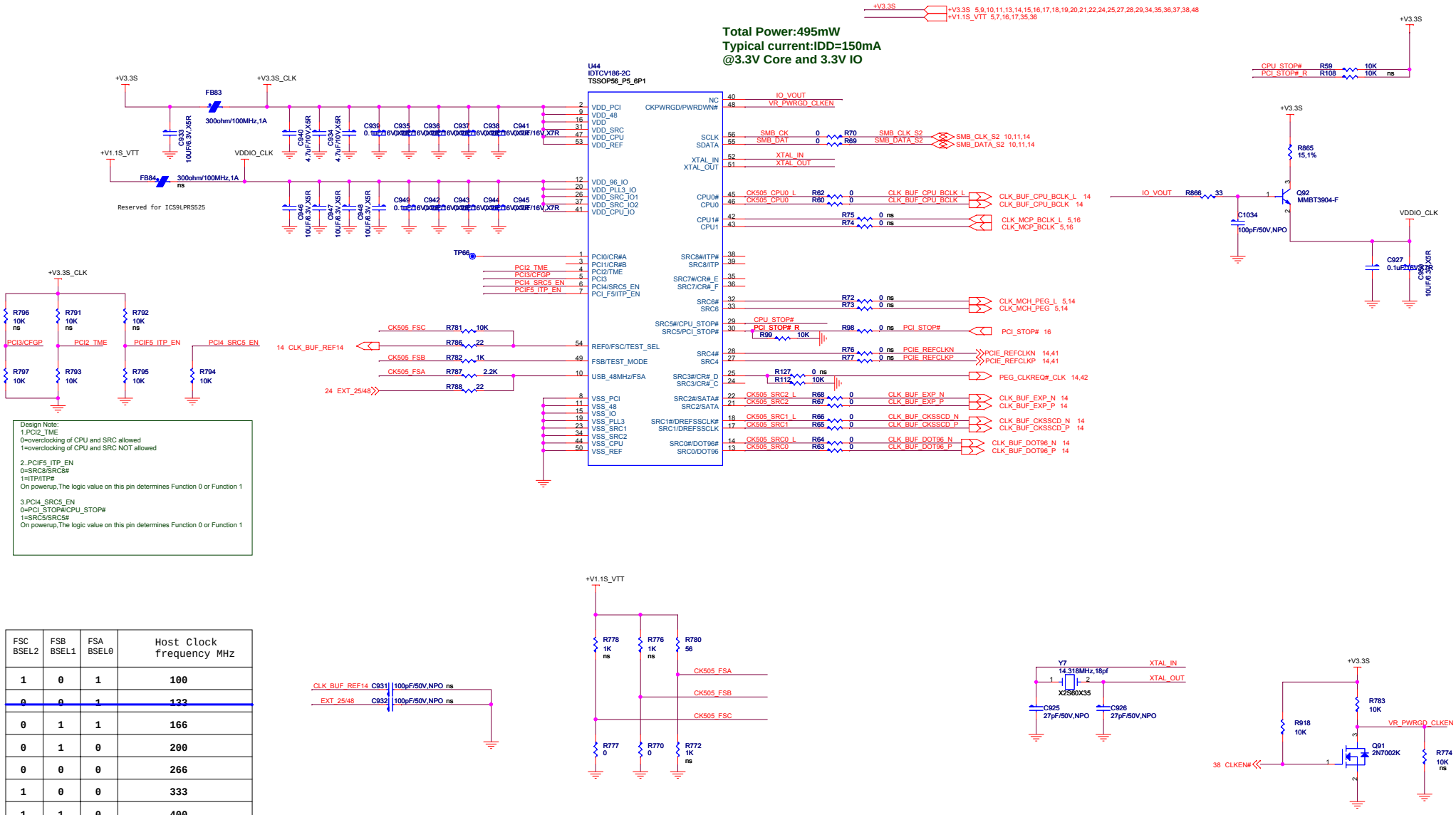

FSC BSEL2	FSB BSEL1	FSA BSEL0	Host Clock frequency MHz
1	0	1	100
0	0	1	133
0	1	1	166
0	1	0	200
0	0	0	266
1	0	0	333
1	1	0	400
1	1	1	Reserved

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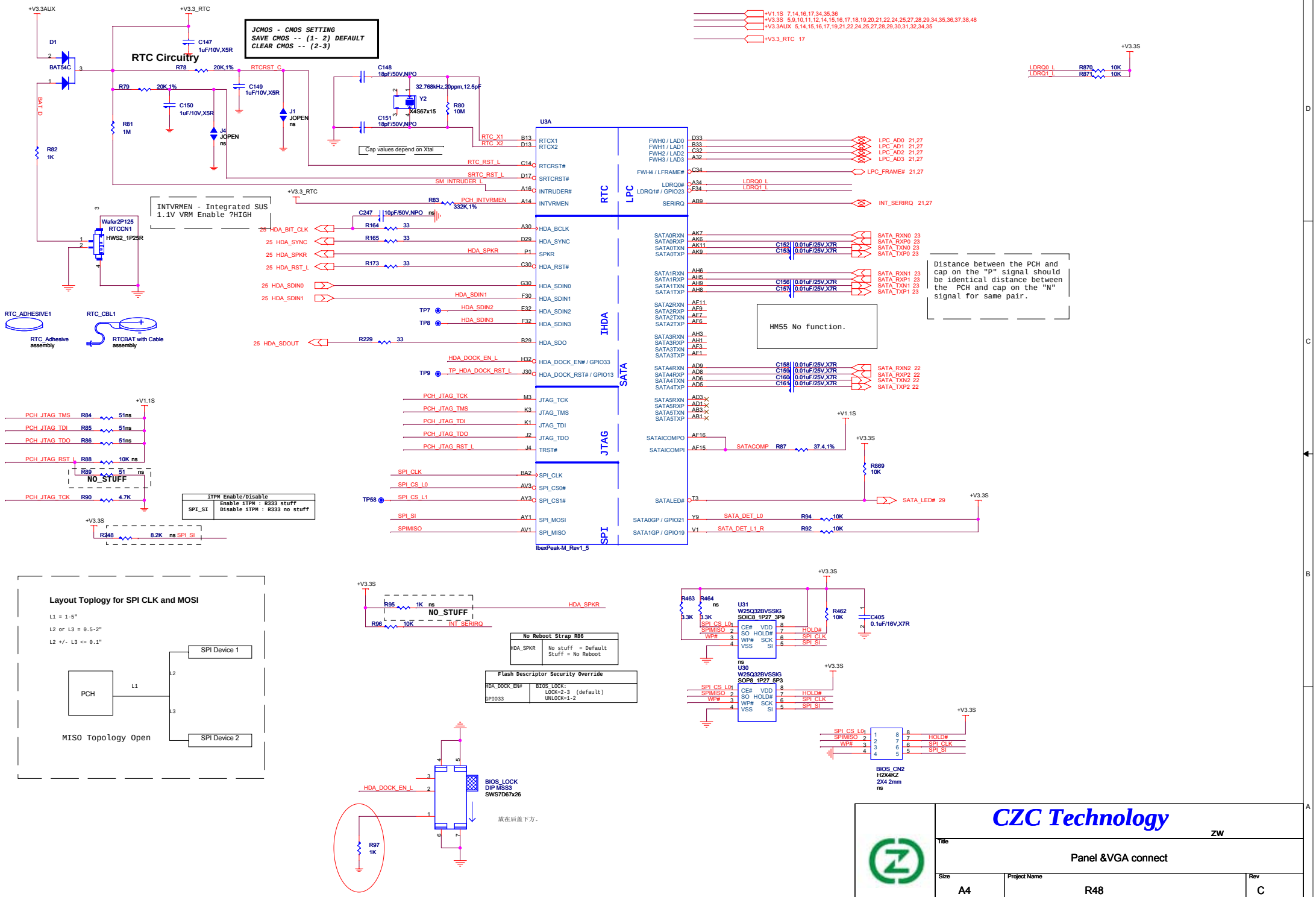
RTC Circuitry
JCMOS - CMOS SETTING
SAVE CMOS -- (1- 2) DEFAULT
CLEAR CMOS -- (2-3)
INTVRMEN - Integrated SUS 1.1V VRM Enable ?HIGH
Cap values depend on Xtal
Distance between the PCH and cap on the "P" signal should be identical distance between the PCH and cap on the "N" signal for same pair.
HM55 No function.
NO_STUFF
iTPM Enable/Disable
Enable iTPM : R333 stuff
Disable iTPM : R333 no stuff
No Reboot Strap R86
Flash Descriptor Security Override
Layout Toplogy for SPI CLK and MOSI
L1 = 1-5"
L2 or L3 = 0.5-2"
L2 +/- L3 <= 0.1"
PCH
SPI Device 1
SPI Device 2
MISO Topology Open
U3A
RTC
LPC
IHDA
SATA
JTAG
SPI
ibexPeak-M_Rev1_5
U31
W25Q32BVSSIG
SOIC8_1P27_3P9
U30
W25Q32BVSSIG
SOP8_1P27_5P3
BIOS_CN2
H2X4KZ
2X4 2mm
BIOS_LOCK
DIP MSS3
SWS7D67x26
放在后盖下方。
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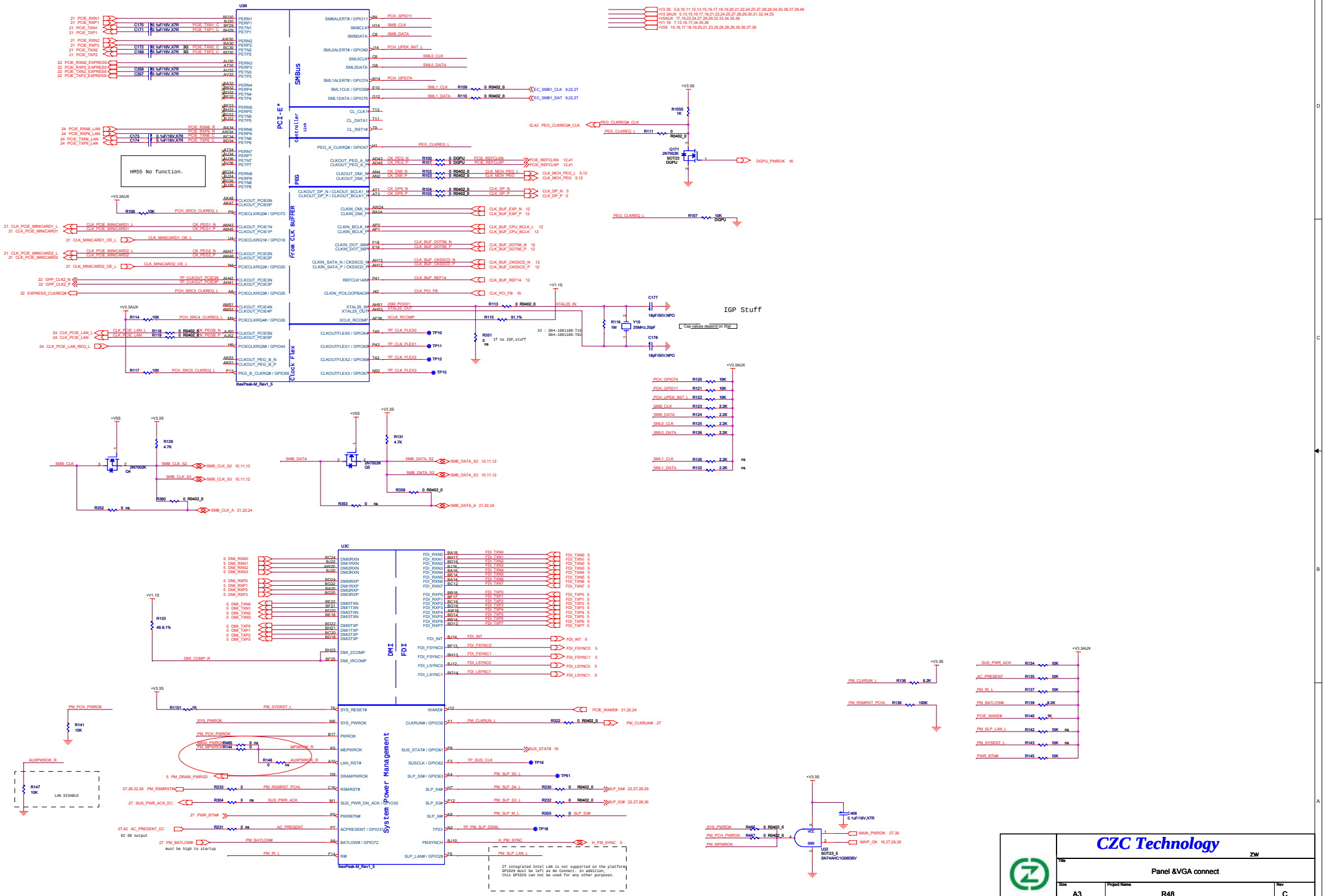
U3B
PCI-E*
SMBUS
Controller
LAN
PEG
From CLK BUFFER
Clock Flex
HM55 No function.
IbexPeak-M_Rev1_5
IGP Stuff
U3C
DMI
FDI
System Power Management
LAN DISABLE
If integrated Intel LAN is not supported on the platform GPIO29 must be left as No Connect. In addition, this GPIO29 can not be used for any other purposes.
must be high to startup
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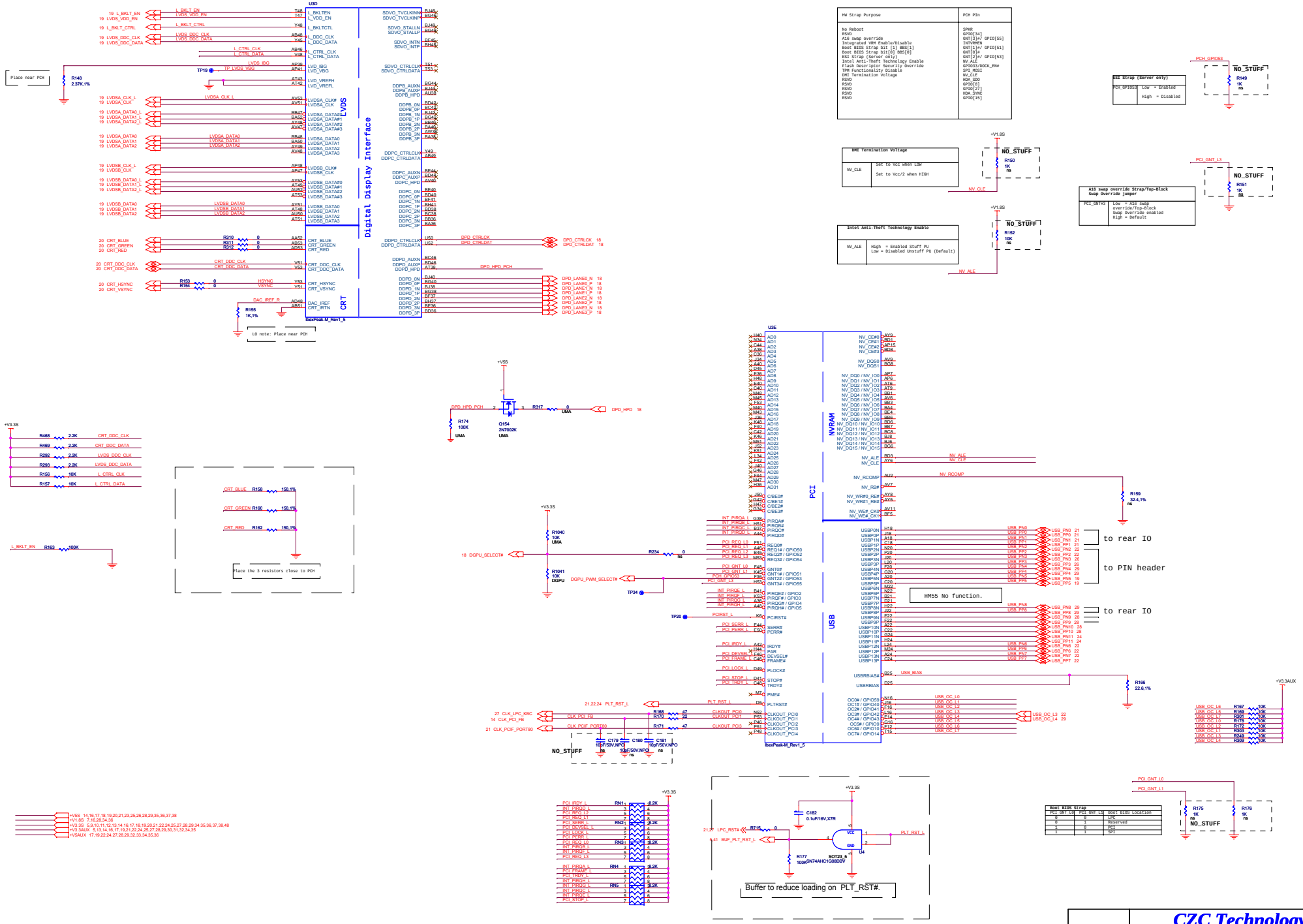

Boot BIOS Strap		
PCI_GNT_L0	PCI_GNT_L1	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI

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Title: Panel &VGA connect

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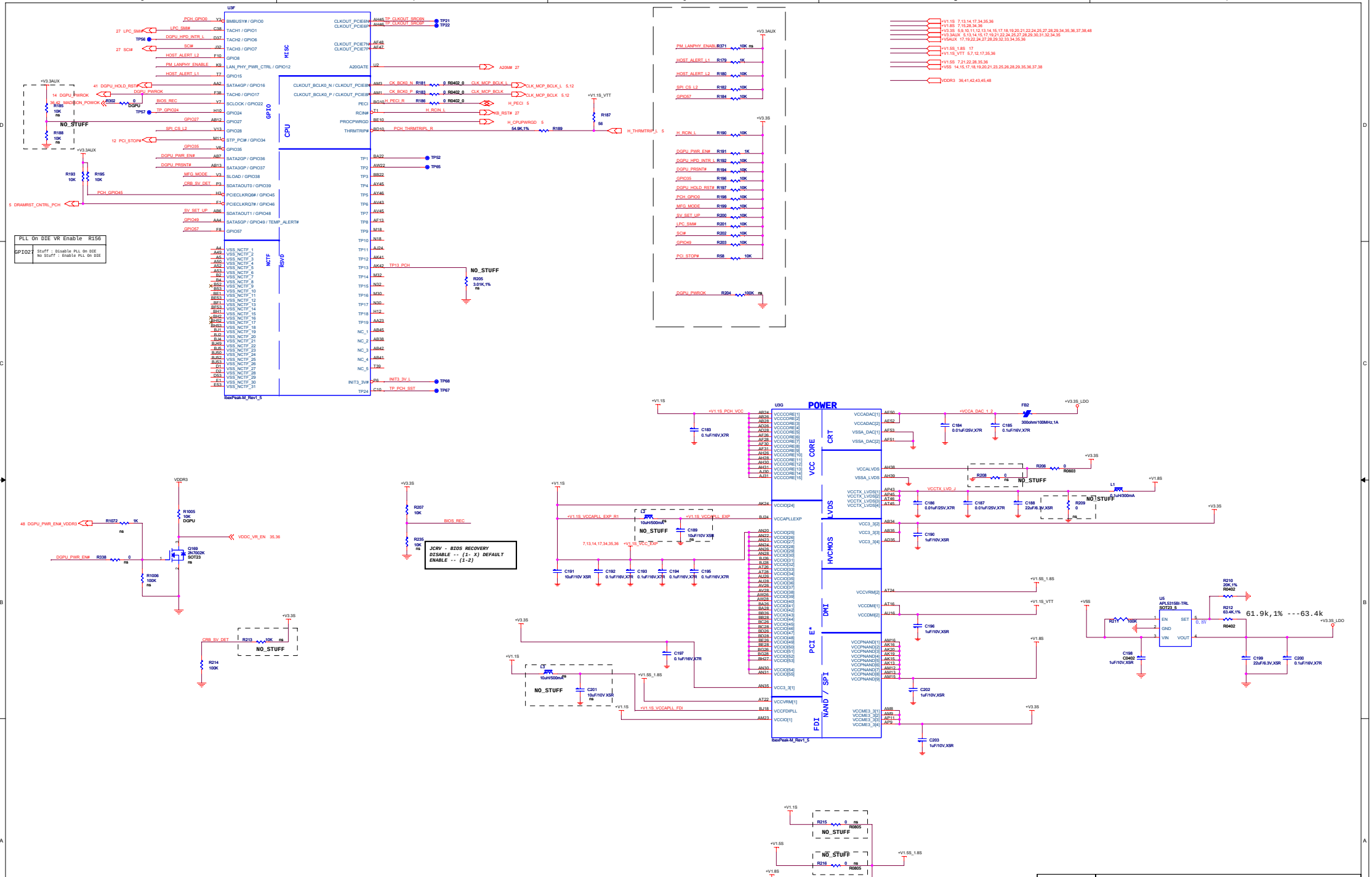
U3F
KI,SC
GPIO
CPU
NCTF
Rsv'd
PLL On DIE VR Enable R156
GPIO27 Stuff : Disable PLL On DIE
No Stuff : Enable PLL On DIE
NO_STUFF
U3G
POWER
VCC CORE
CRT
LVDS
HVCMOS
DMI
PCI E*
NAND / SPI
FDI
JCRV - BIOS RECOVERY
DISABLE -- (1- X) DEFAULT
ENABLE -- (1-2)
U5
APL5315BI-TRL
SOT23_5
61.9k,1% ---63.4k
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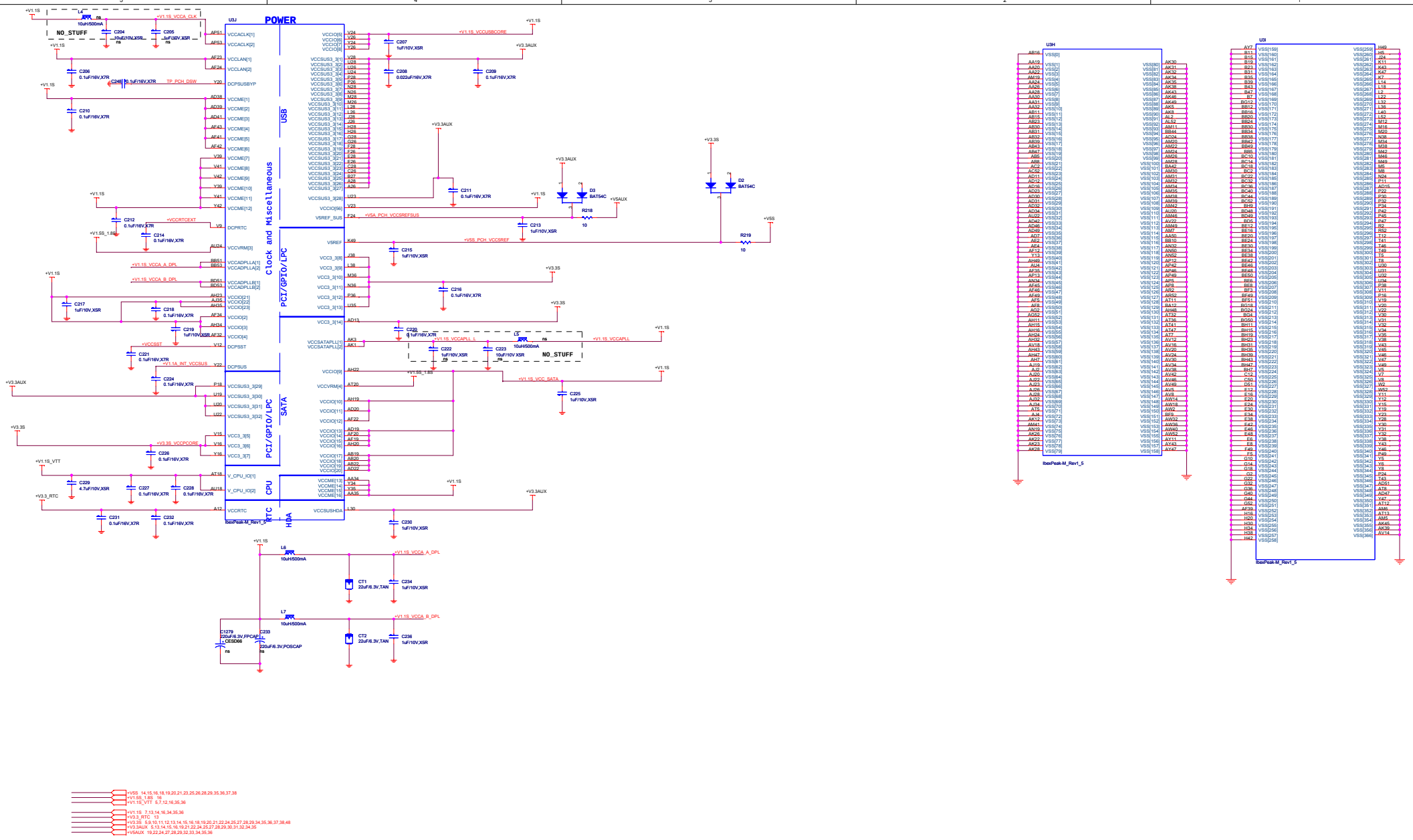

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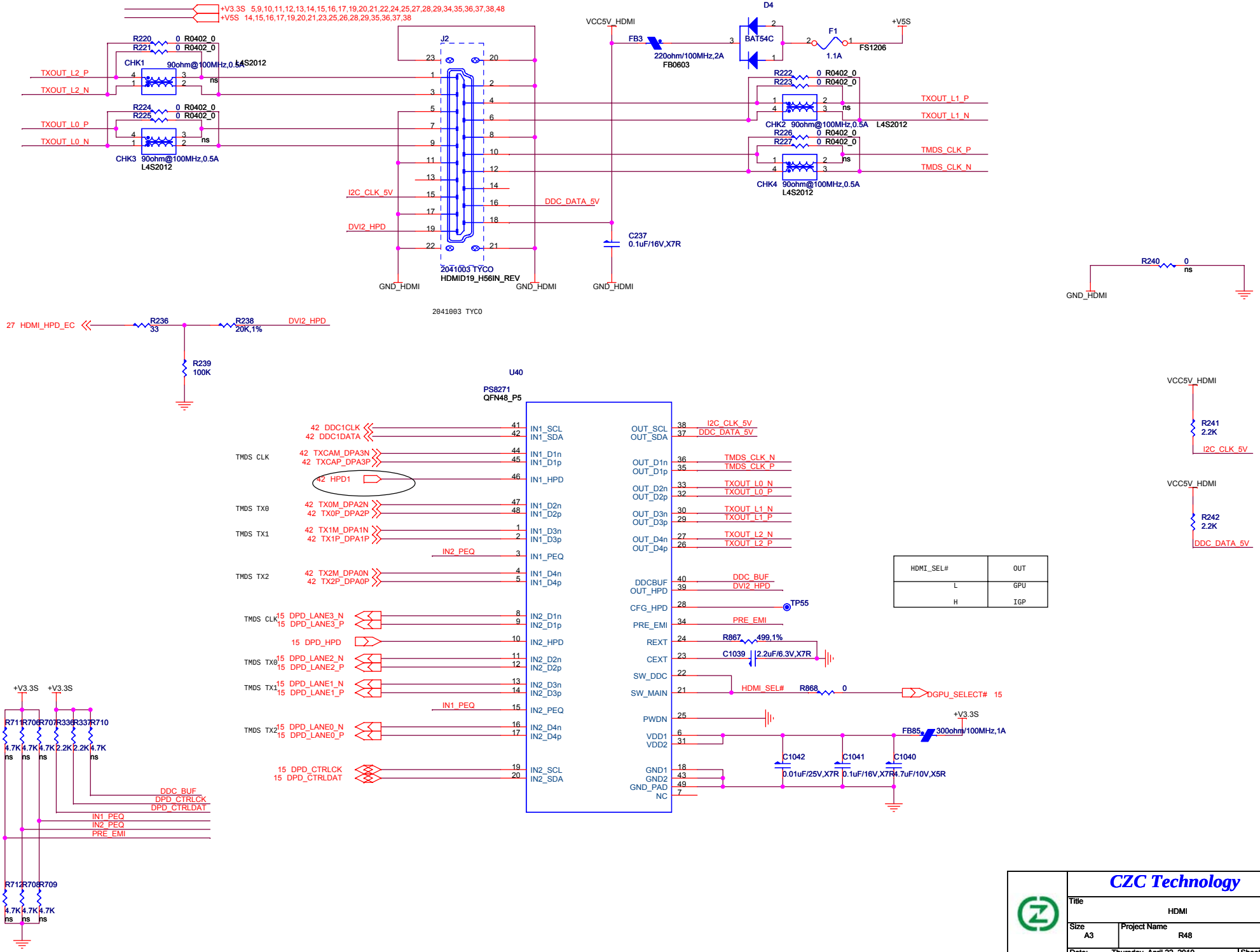

HDMI_SEL#	OUT
L	GPU
H	IGP

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Title: HDMI

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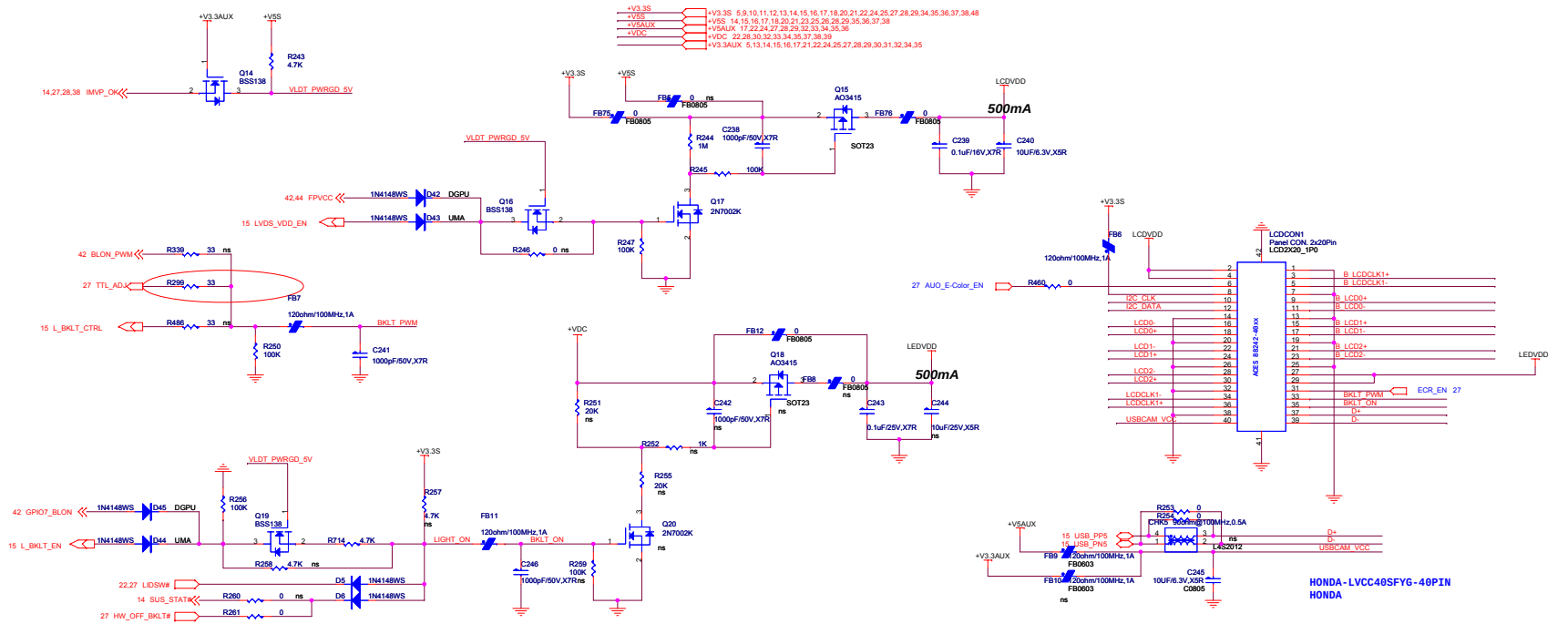
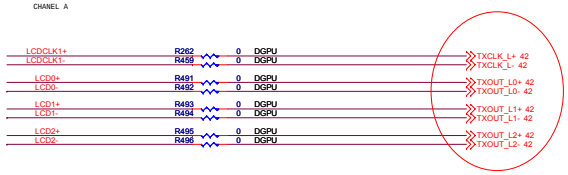
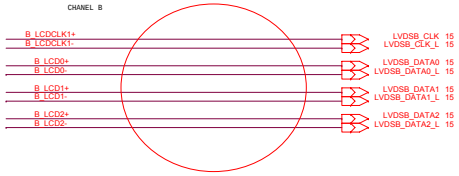


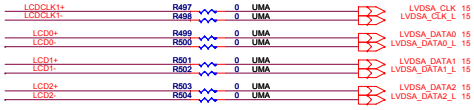
LVDS_SEL#	OUT
L	GPU
H	IGP

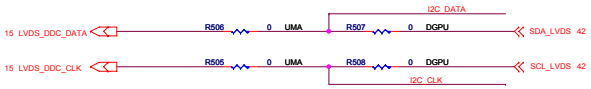
CHANEL A



CHANEL B



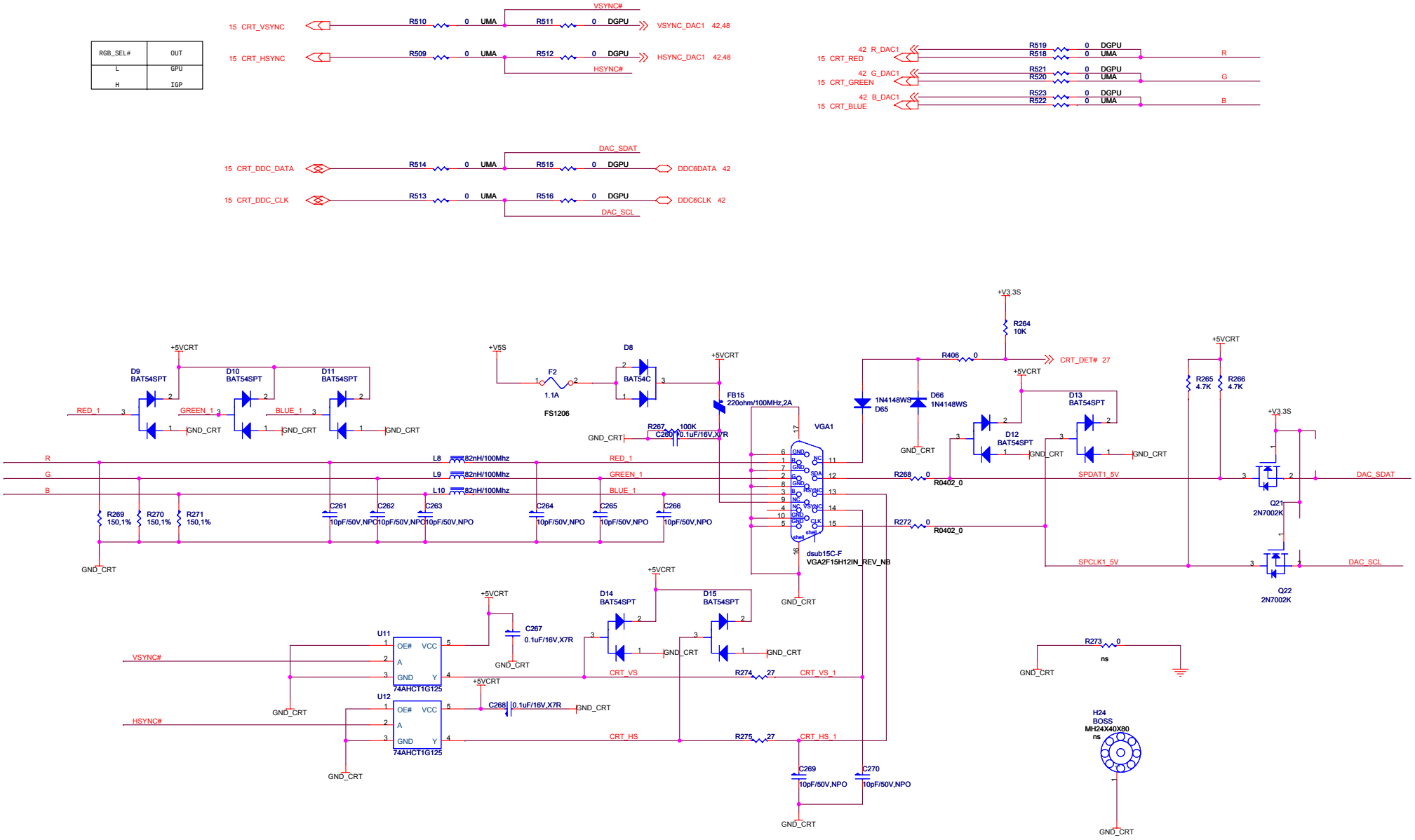




CZC Technology

Title	Panel &VGA connect		zw
Size: Custom	Project Name: R48		Rev: C
Date: Thursday, April 22, 2010	Sheet 19 of 56		

RGB_SEL#	OUT
L	GPU
H	IGP



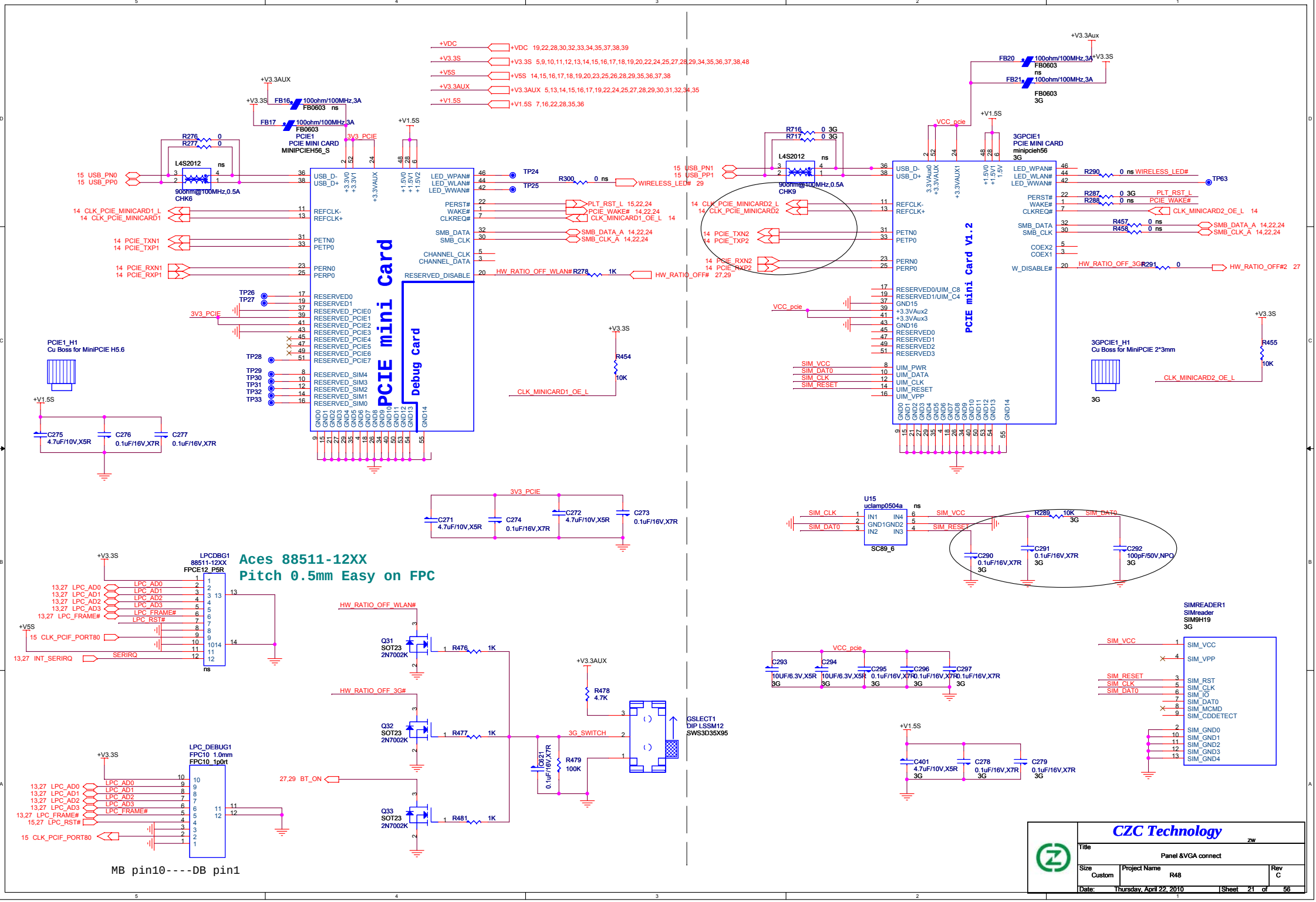
CZC Technology

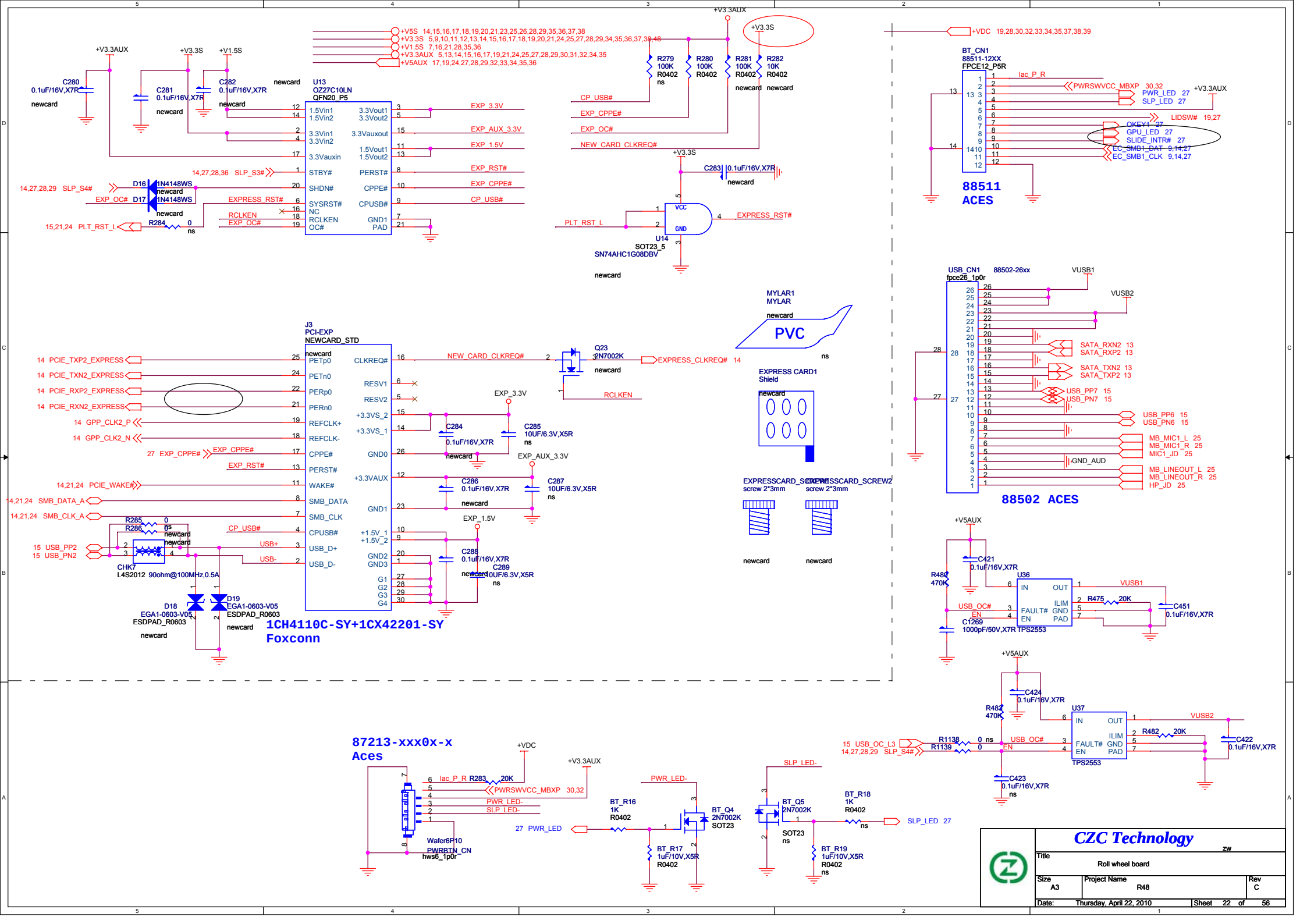
zw

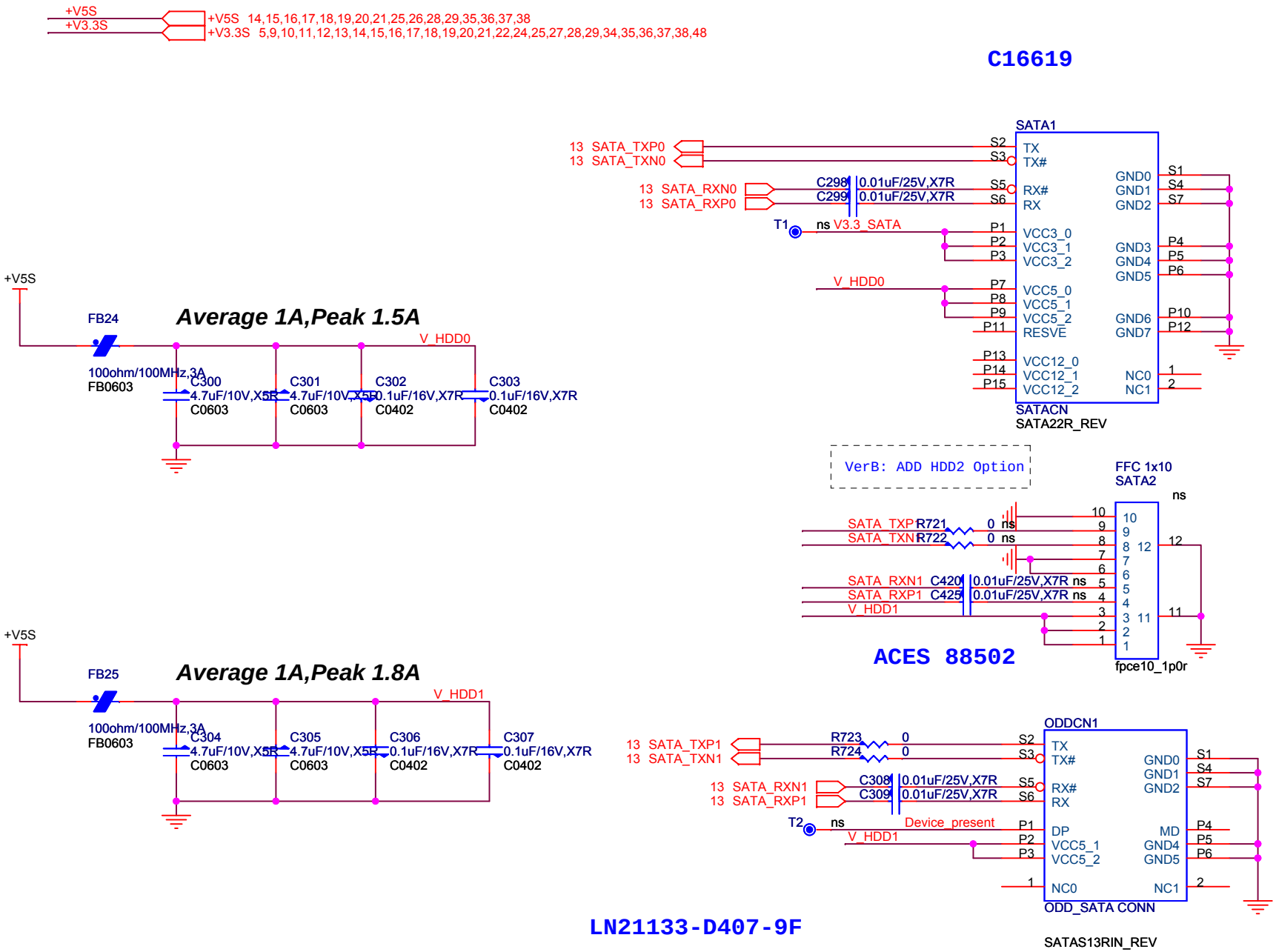
Title: Panel &VGA connect

Size: Custom | Project Name: R48 | Rev: C

Date: Thursday, April 22, 2010 | Sheet 20 of 56


PCIE mini Card
Debug Card
PCIE mini Card V1.2
PCIE1
PCIE MINI CARD
MINIPCIEH56_S
3GPCIE1
PCIE MINI CARD
minipcieh56
3G
PCIE1_H1
Cu Boss for MiniPCIE H5.6
3GPCIE1_H1
Cu Boss for MiniPCIE 2*3mm
Aces 88511-12XX
Pitch 0.5mm Easy on FPC
LPCDBG1
88511-12XX
FPCE12_P5R
LPC_DEBUG1
FPC10 1.0mm
FPC10 1p0rt
MB pin10----DB pin1
U15
uclamp0504a
SC89_6
SIMREADER1
SIMreader
SIM9H19
GSLECT1
DIP LSSM12
SWS3D35X95
CZC Technology
Panel &VGA connect
Size
Custom
Project Name
R48
Rev
C
Date:
Thursday, April 22, 2010
Sheet 21 of 56


U13
OZ27C10LN
QFN20_P5
1.5Vin1
1.5Vin2
3.3Vin1
3.3Vin2
3.3Vauxin
STBY#
SHDN#
SYSRST#
NC
RCLKEN
OC#
3.3Vout1
3.3Vout2
3.3Vauxout
1.5Vout1
1.5Vout2
PERST#
CPPE#
CPUSB#
GND1
PAD
EXP_3.3V
EXP_AUX_3.3V
EXP_1.5V
EXP_RST#
EXP_CPPE#
CP_USB#
SLP_S3#
SLP_S4#
EXPRESS_RST#
PLT_RST_L
D16 1N4148WS
D17 1N4148WS
R284 0 ns
C280 0.1uF/16V,X7R
C281 0.1uF/16V,X7R
C282 0.1uF/16V,X7R
newcard
+V3.3AUX
+V3.3S
+V1.5S
+V5S 14,15,16,17,18,19,20,21,23,25,26,28,29,35,36,37,38
+V3.3S 5,9,10,11,12,13,14,15,16,17,18,19,20,21,24,25,27,28,29,34,35,36,37,38,48
+V1.5S 7,16,21,28,35,36
+V3.3AUX 5,13,14,15,16,17,19,21,24,25,27,28,29,30,31,32,34,35
+V5AUX 17,19,24,27,28,29,32,33,34,35,36
R279 100K R0402 ns
R280 100K R0402
R281 100K R0402
R282 10K R0402
NEW_CARD_CLKREQ#
C283 0.1uF/16V,X7R
U14
SOT23_5
SN74AHC1G08DBV
VCC
GND
EXPRESS_RST#
PLT_RST_L
+VDC 19,28,30,32,33,34,35,37,38,39
BT_CN1
88511-12XX
FPCE12_P5R
Iac_P_R
PWRSWVCC_MBXP 30,32
PWR_LED 27
SLP_LED 27
LIDSW# 19,27
OKEY1 27
GPU_LED 27
SLIDE_INTR# 27
EC_SMB1_DAT 9,14,27
EC_SMB1_CLK 9,14,27
88511
ACES
J3
PCI-EXP
NEWCARD_STD
PETp0
PETn0
PERp0
PERn0
REFCLK+
REFCLK-
CPPE#
PERST#
WAKE#
SMB_DATA
SMB_CLK
CPUSB#
USB_D+
USB_D-
CLKREQ#
RESV1
RESV2
+3.3VS_2
+3.3VS_1
GND0
+3.3VAUX
GND1
+1.5V_1
+1.5V_2
GND2
GND3
G1
G2
G3
G4
14 PCIE_TXP2_EXPRESS
14 PCIE_TXN2_EXPRESS
14 PCIE_RXP2_EXPRESS
14 PCIE_RXN2_EXPRESS
14 GPP_CLK2_P
14 GPP_CLK2_N
27 EXP_CPPE#
14,21,24 PCIE_WAKE#
14,21,24 SMB_DATA_A
14,21,24 SMB_CLK_A
15 USB_PP2
15 USB_PN2
USB+
USB-
R285 0 ns
R286 0 ns
CHK7
L4S2012 90ohm@100MHz,0.5A
D18 EGA1-0603-V05 ESDPAD_R0603
D19 EGA1-0603-V05 ESDPAD_R0603
NEW_CARD_CLKREQ#
Q23 2N7002K
EXPRESS_CLKREQ# 14
RCLKEN
C284 0.1uF/16V,X7R
C285 10UF/6.3V,X5R ns
C286 0.1uF/16V,X7R
C287 10UF/6.3V,X5R ns
C288 0.1uF/16V,X7R
C289 10UF/6.3V,X5R ns
1CH4110C-SY+1CX42201-SY
Foxconn
MYLAR1
MYLAR
PVC
EXPRESS CARD1
Shield
EXPRESSCARD_SCREW1
EXPRESSCARD_SCREW2
screw 2*3mm
USB_CN1
fpce26_1p0r
88502-26xx
VUSB1
VUSB2
SATA_RXN2 13
SATA_RXP2 13
SATA_TXN2 13
SATA_TXP2 13
USB_PP7 15
USB_PN7 15
USB_PP6 15
USB_PN6 15
MB_MIC1_L 25
MB_MIC1_R 25
MIC1_JD 25
GND_AUD
MB_LINEOUT_L 25
MB_LINEOUT_R 25
HP_JD 25
88502 ACES
+V5AUX
C421 0.1uF/16V,X7R
R480 470K
U36
TPS2553
IN
OUT
ILIM
FAULT#
EN
GND
PAD
R475 20K
C451 0.1uF/16V,X7R
USB_OC#
C1269 1000pF/50V,X7R
C424 0.1uF/16V,X7R
R482 470K
U37
R482 20K
C422 0.1uF/16V,X7R
C423 0.1uF/16V,X7R ns
15 USB_OC_L3
14,27,28,29 SLP_S4#
R1138 0 ns
R1139 0
87213-xxx0x-x
Aces
Wafer6P10
PWRBTN_CN
hws6_1p0r
Iac_P_R R283 20K
PWRSWVCC_MBXP 30,32
PWR_LED-
SLP_LED-
+VDC
+V3.3AUX
BT_R16 1K R0402
BT_R17 1uF/10V,X5R R0402
BT_Q4 2N7002K SOT23
27 PWR_LED
BT_Q5 2N7002K
SOT23 ns
BT_R18 1K R0402 ns
BT_R19 1uF/10V,X5R R0402 ns
SLP_LED 27
CZC Technology
zw
Title
Roll wheel board
Size
A3
Project Name
R48
Rev
C
Date: Thursday, April 22, 2010
Sheet 22 of 56

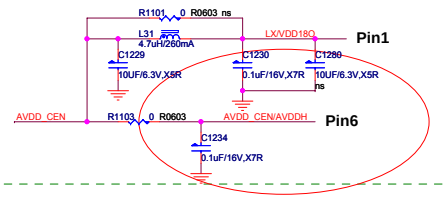


CZC Technology	zw	
Title: SATA HDD ODD		
Size: A4	Project Name: R48	Rev: C
Date: Thursday, April 22, 2010	Sheet 23 of 56	

AR8131/M, 8121 GigaBit Lan
AR8132/M, 8114 10M/100M Lan

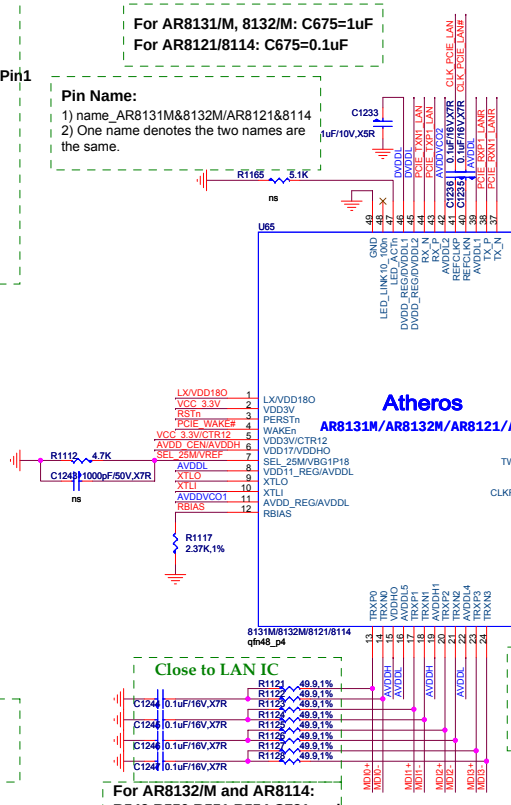
Close to U26

For AR8131/M, 8132/M: remove R348, C325. C337=0.1uF
For AR8121/8114: remove L9, C306, R322. C337=1uF. C325 close to Pin1

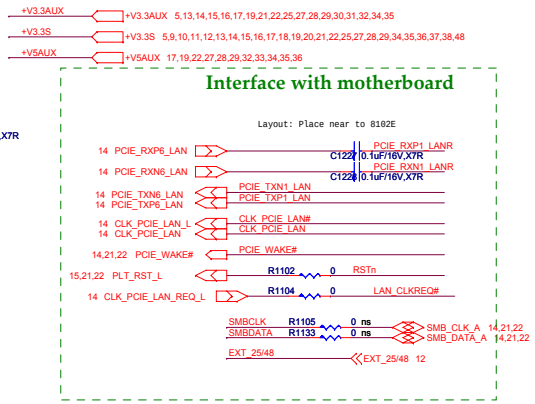


For AR8131/M, 8132/M: C675=1uF
For AR8121/8114: C675=0.1uF

Pin Name:
1) name_AR8131M&8132M/AR8121&8114
2) One name denotes the two names are the same.

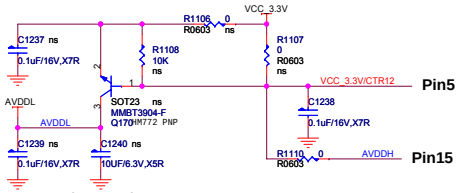


C683 close to Pin30
For AR8131/8132: Remove C683



For AR8121/8114: Remove R335
CLKREQn/PNP_PWR_SEL R1109 0 LAN_CLKREQ#

For AR8121/8114: Pin27 power-on strapping (internal pull- up for input)
If R341 and R343 are removed, Q1 collector connects 3.3V and remove R327.
If R341 is removed ,and R343 is stuffed, Q1 collector connects 1.8V and remove R328.



For AR8131/M, 8132/M:
option1: remove R328, R327, R349, R334, C302, C342, C311, Q7.
option2: remove R328, R327, R349, R339, C302, C342, C311, Q7.

For AR8121/8114: remove C320, R339
Q7 close to Pin8

Clock Resource

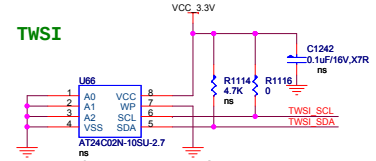
For AR8121/8114 : Remove R336
For AR8131/M, 8132/M Input 25M: Remove R336, C339
For AR8131/M, 8132/M Input 48M: Stuff R336. Remove C339

Close to LAN IC

For AR8132/M and AR8114:
R549,R550,R551,R554,C731 and C732 can be removed.

R6,R8,R13 and R14 are pull-up resistors, which might not be necessary due to existence on motherboard.

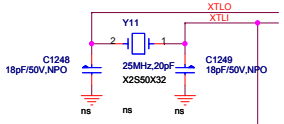
TWSI



For AR8131M/8132M: R340=0 ohm. Remove U12, C301, R344.
For AR8131/8132 eeprom application, reserve TWSI circuit.

Pin6 AVDD_CEN/AVDDH R1120 0 R0603 ns AVDDH
For AR8131/M, AR8132/M: Remove R342

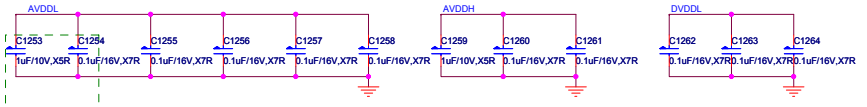
25MHz Crystal



External clock

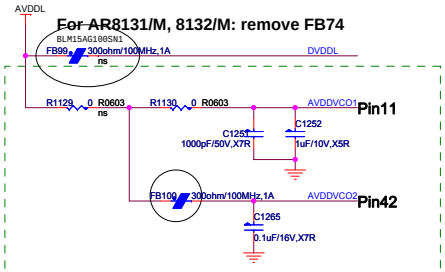
EXT_25/48 10pF/50V,NPO C1250

For AR8121/8114 : Remove C322
For AR8131/M, 8132/M intertnal clock: Remove C322
For AR8131/M, 8132/M external clock: Remove Y4, C687, C688
If the external clock is swing from 0 to 0.8V, EXT_25/48 can be connected to XTLI directly.

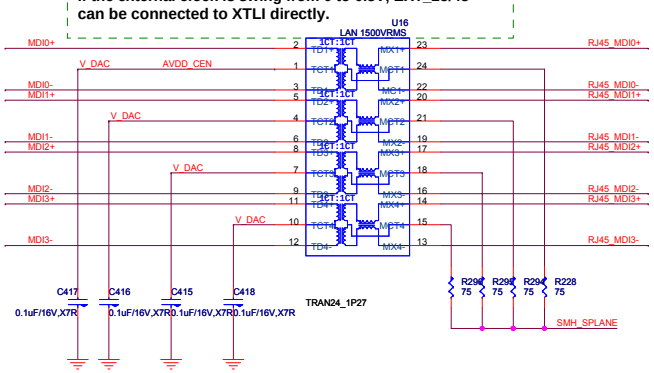


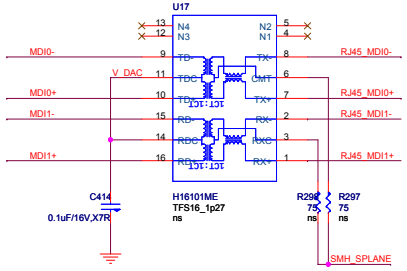
C684, C685 close to Pin8

For AR8131/M, 8132/M: remove FB74

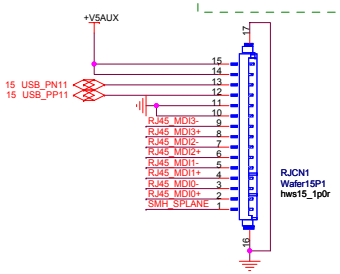


If overclocking, R332, FB75 stuffed and R330 removed.
If not overclocking, R330, FB75 stuffed and R332 removed.
For AR8131/M, AR8132/M: FB75 can be 0 ohm



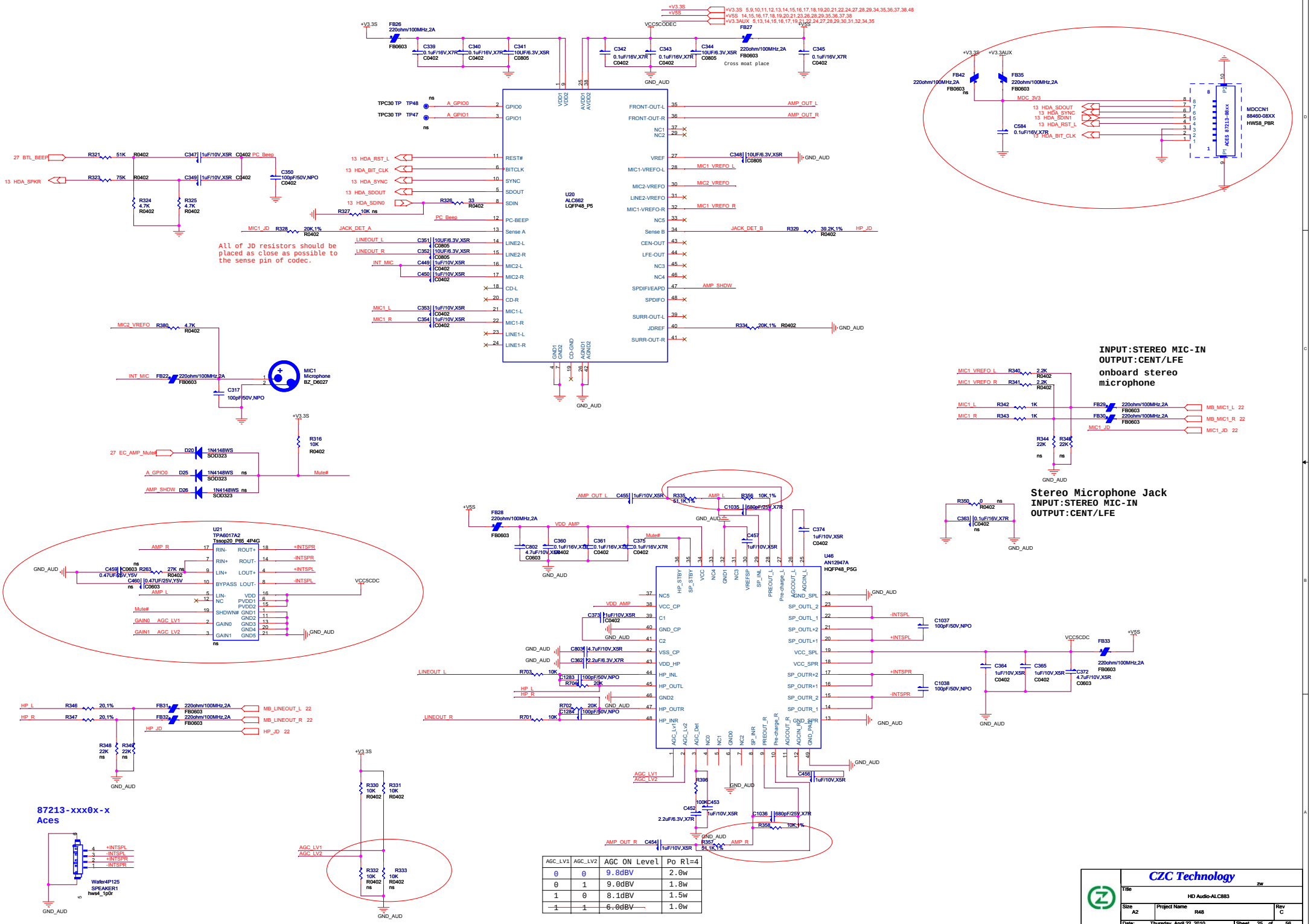


87213-xxx0x-x
ACES

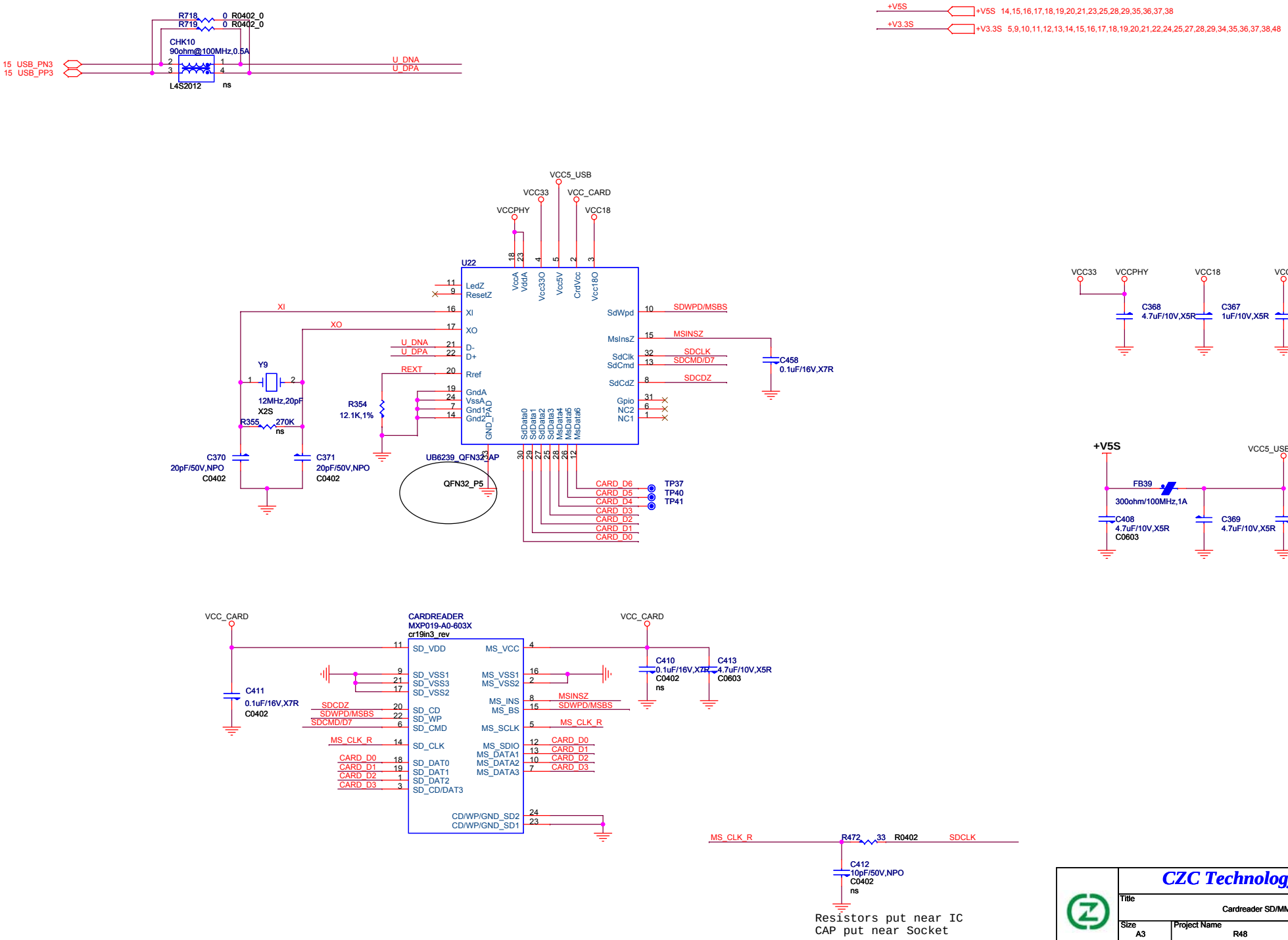


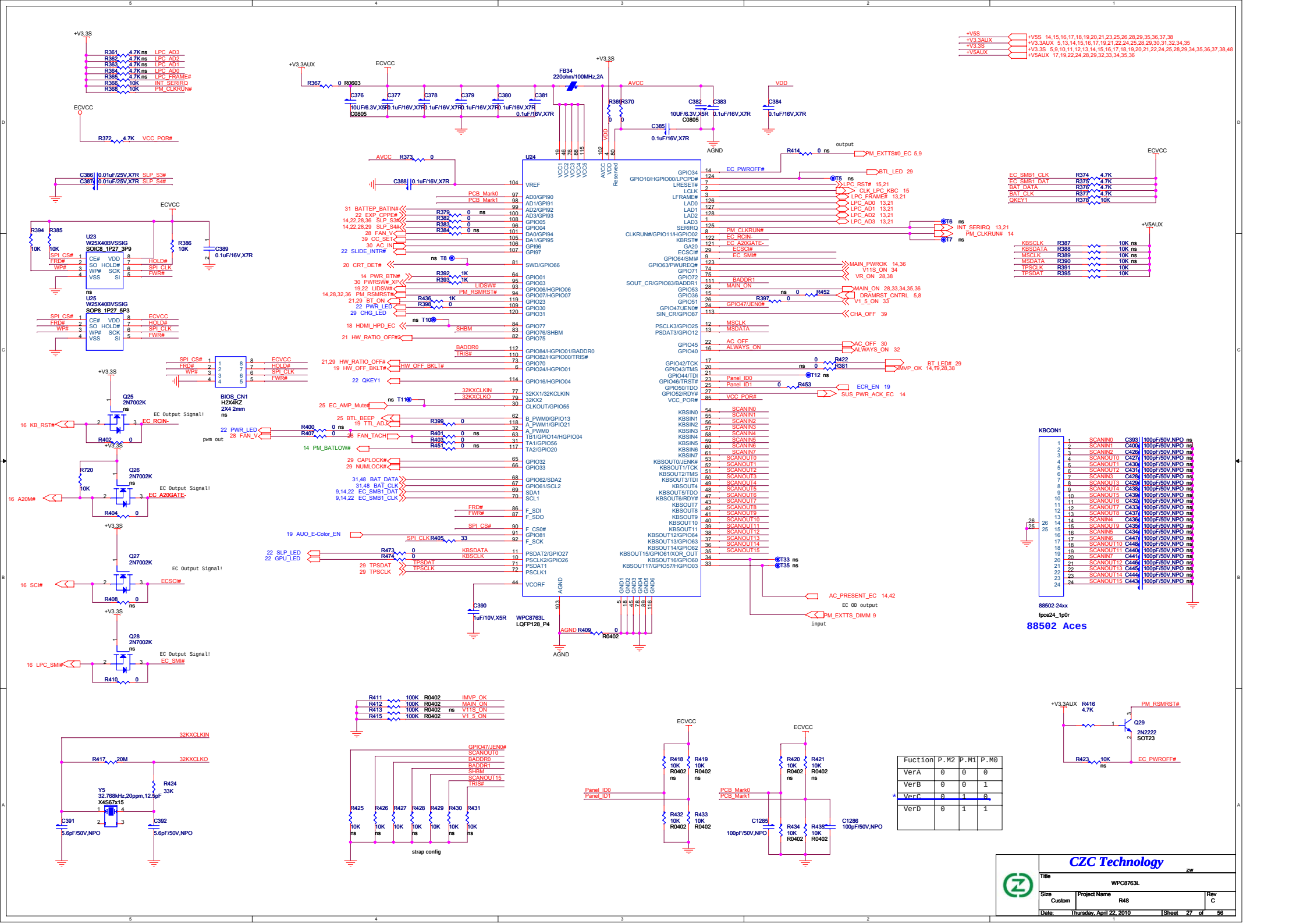
CZC Technology

Title: LAN		zw
Size: C	Project Name: R48	Rev: C
Date: Thursday, April 22, 2010	Sheet 24 of 56	

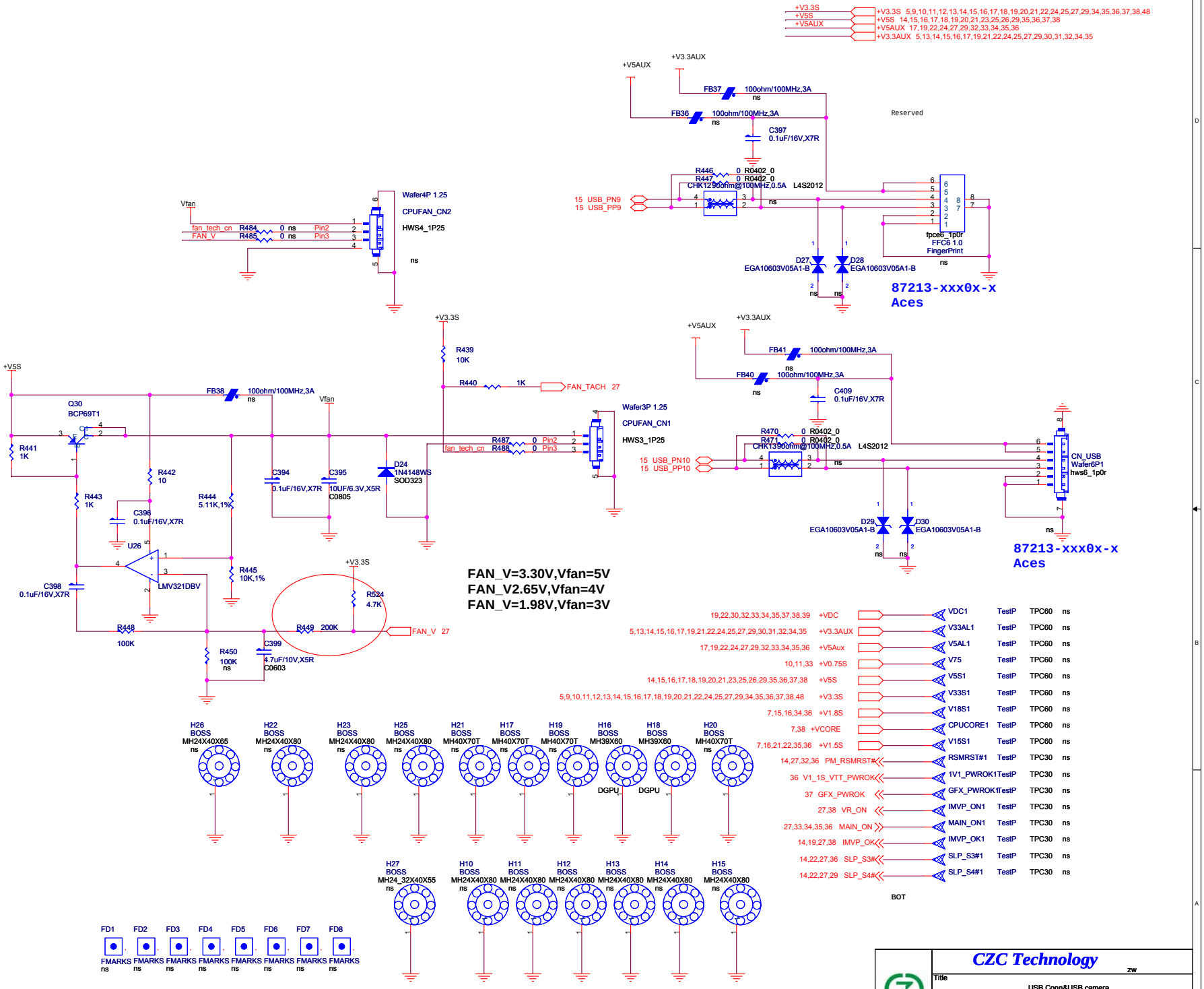


AGC_LV1	AGC_LV2	AGC ON Level	Po Rl=4
0	0	9.8dBV	2.0w
0	1	9.0dBV	1.8w
1	0	8.1dBV	1.5w
1	1	6.0dBV	1.0w

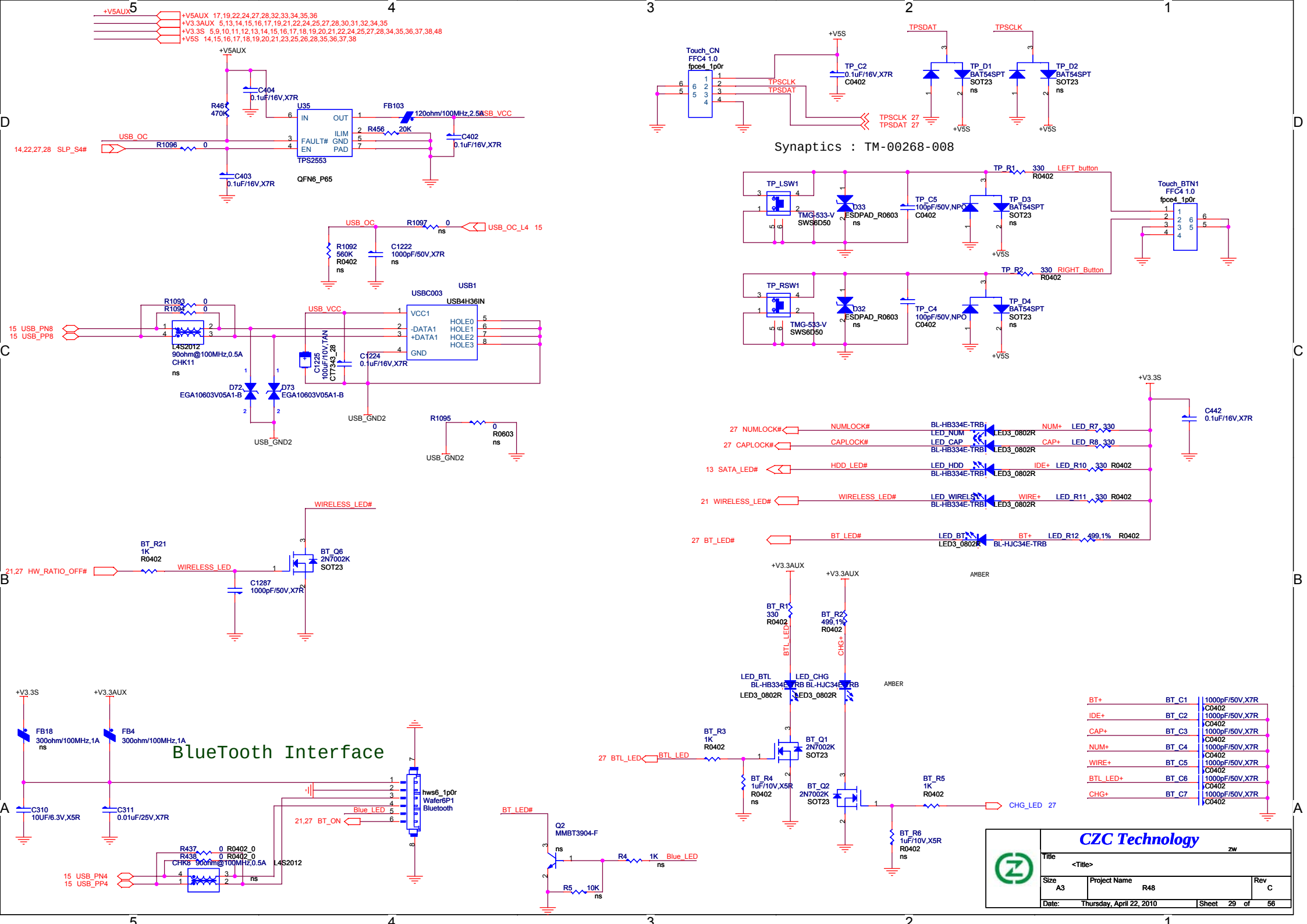

R718 0 R0402_0
R719 0 R0402_0
CHK10
90ohm@100MHz,0.5A
L4S2012
ns
15 USB_PN3
15 USB_PP3
U_DNA
U_DPA
+V5S
+V5S 14,15,16,17,18,19,20,21,23,25,28,29,35,36,37,38
+V3.3S
+V3.3S 5,9,10,11,12,13,14,15,16,17,18,19,20,21,22,24,25,27,28,29,34,35,36,37,38,48
VCC5_USB
VCC33
VCC_CARD
VCCPHY
VCC18
U22
LedZ
ResetZ
XI
XO
D-
D+
Rref
GndA
VssA
Gnd1
Gnd2
GND_PAD
VccA
VddA
Vcc33O
Vcc5V
CrdVcc
Vcc18O
SdWpd
MsInsZ
SdClk
SdCmd
SdCdZ
Gpio
NC2
NC1
SDWPD/MSBS
MSINSZ
SDCLK
SDCMD/D7
SDCDZ
C458
0.1uF/16V,X7R
Y9
12MHz,20pF
X2S
R355 270K
ns
R354
12.1K,1%
REXT
C370
20pF/50V,NPO
C0402
C371
20pF/50V,NPO
C0402
UB6239_QFN32_CAP
QFN32_P5
SdData0
SdData1
SdData2
SdData3
MsData4
MsData5
MsData6
CARD_D6
CARD_D5
CARD_D4
CARD_D3
CARD_D2
CARD_D1
CARD_D0
TP37
TP40
TP41
VCC33
VCCPHY
VCC18
VCC_CARD
C368
4.7uF/10V,X5R
C367
1uF/10V,X5R
C366
4.7uF/10V,X5R
+V5S
VCC5_USB
FB39
300ohm/100MHz,1A
C408
4.7uF/10V,X5R
C0603
C369
4.7uF/10V,X5R
C407
0.1uF/16V,X7R
VCC_CARD
CARDREADER
MXP019-A0-603X
cr19in3_rev
SD_VDD
SD_VSS1
SD_VSS3
SD_VSS2
SD_CD
SD_WP
SD_CMD
SD_CLK
SD_DAT0
SD_DAT1
SD_DAT2
SD_CD/DAT3
MS_VCC
MS_VSS1
MS_VSS2
MS_INS
MS_BS
MS_SCLK
MS_SDIO
MS_DATA1
MS_DATA2
MS_DATA3
CD/WP/GND_SD2
CD/WP/GND_SD1
SDCDZ
SDWPD/MSBS
SDCMD/D7
MS_CLK_R
CARD_D0
CARD_D1
CARD_D2
CARD_D3
MSINSZ
C411
0.1uF/16V,X7R
C0402
C410
0.1uF/16V,X7R
C0402
ns
C413
4.7uF/10V,X5R
C0603
MS_CLK_R
R472 33 R0402
SDCLK
C412
10pF/50V,NPO
C0402
ns
Resistors put near IC
CAP put near Socket
CZC Technology
Title
Cardreader SD/MMC/MS
Size
A3
Project Name
R48
Rev
C
Date: Thursday, April 22, 2010
Sheet 26 of 56



Fuction	P.M2	P.M1	P.M0
VerA	0	0	0
VerB	0	0	1
* VerC	0	1	0
VerD	0	1	1



CZC Technology	zw
Title	USB Conn&USB camera
Size: Custom	Project Name: R48
Rev	C
Date: Thursday, April 22, 2010	Sheet 28 of 56


+V5AUX 17,19,22,24,27,28,32,33,34,35,36
+V3.3AUX 5,13,14,15,16,17,19,21,22,24,25,27,28,30,31,32,34,35
+V3.3S 5,9,10,11,12,13,14,15,16,17,18,19,20,21,22,24,25,27,28,34,35,36,37,38,48
+V5S 14,15,16,17,18,19,20,21,23,25,26,28,35,36,37,38
U35
TPS2553
QFN6_P65
FB103
120ohm/100MHz,2.5A
USB_VCC
USB_OC
14,22,27,28 SLP_S4#
USB_OC_L4 15
USBC003
USB4H36IN
USB1
15 USB_PN8
15 USB_PP8
L4S2012
90ohm@100MHz,0.5A
CHK11
D72 EGA10603V05A1-B
D73 EGA10603V05A1-B
USB_GND2
WIRELESS_LED#
BT_R21 1K R0402
21,27 HW_RATIO_OFF#
WIRELESS_LED
BT_Q6 2N7002K SOT23
C1287 1000pF/50V,X7R
Touch_CN FFC4 1.0 fpce4_1p0r
TPSCLK
TPSDAT
TPSCLK 27
TPSDAT 27
TP_C2 0.1uF/16V,X7R C0402
TP_D1 BAT54SPT SOT23 ns
TP_D2 BAT54SPT SOT23 ns
Synaptics : TM-00268-008
TP_LSW1
TMG-533-V SWS6D50
D33 ESDPAD_R0603 ns
TP_C5 100pF/50V,NPO C0402
TP_D3 BAT54SPT SOT23 ns
TP_R1 330 R0402
LEFT_button
Touch_BTN1 FFC4 1.0 fpce4_1p0r
TP_RSW1
D32 ESDPAD_R0603 ns
TP_C4 100pF/50V,NPO C0402
TP_D4 BAT54SPT SOT23 ns
TP_R2 330 R0402
RIGHT_Button
C442 0.1uF/16V,X7R
27 NUMLOCK#
27 CAPLOCK#
13 SATA_LED#
21 WIRELESS_LED#
27 BT_LED#
LED_NUM BL-HB334E-TRB
LED_CAP BL-HB334E-TRB
LED_HDD BL-HB334E-TRB
LED_WIRELESS BL-HB334E-TRB
LED_BT LED3_0802R
LED_R7 330
LED_R8 330
LED_R10 330 R0402
LED_R11 330 R0402
LED_R12 499,1% R0402
BL-HJC34E-TRB
AMBER
BT_R1 330 R0402
BT_R2 499,1% R0402
LED_BTL BL-HB334E-TRB LED3_0802R
LED_CHG BL-HJC34E-TRB LED3_0802R
BT_R3 1K R0402
27 BTL_LED
BT_Q1 2N7002K SOT23
BT_R4 1uF/10V,X5R R0402 ns
BT_Q2 2N7002K SOT23
BT_R5 1K R0402
BT_R6 1uF/10V,X5R R0402 ns
CHG_LED 27
BT+ BT_C1 1000pF/50V,X7R C0402
IDE+ BT_C2 1000pF/50V,X7R C0402
CAP+ BT_C3 1000pF/50V,X7R C0402
NUM+ BT_C4 1000pF/50V,X7R C0402
WIRE+ BT_C5 1000pF/50V,X7R C0402
BTL_LED+ BT_C6 1000pF/50V,X7R C0402
CHG+ BT_C7 1000pF/50V,X7R C0402
BlueTooth Interface
FB18 300ohm/100MHz,1A ns
FB4 300ohm/100MHz,1A
C310 10UF/6.3V,X5R
C311 0.01uF/25V,X7R
hws6_1p0r Wafer6P1 Bluetooth
Blue_LED
21,27 BT_ON
BT_LED#
Q2 MMBT3904-F ns
R4 1K Blue_LED ns
R5 10K ns
R437 0 R0402_0
R438 0 R0402_0
CHK8 90ohm@100MHz,0.5A
L4S2012
15 USB_PN4
15 USB_PP4
CZC Technology
zw
Title
<Title>
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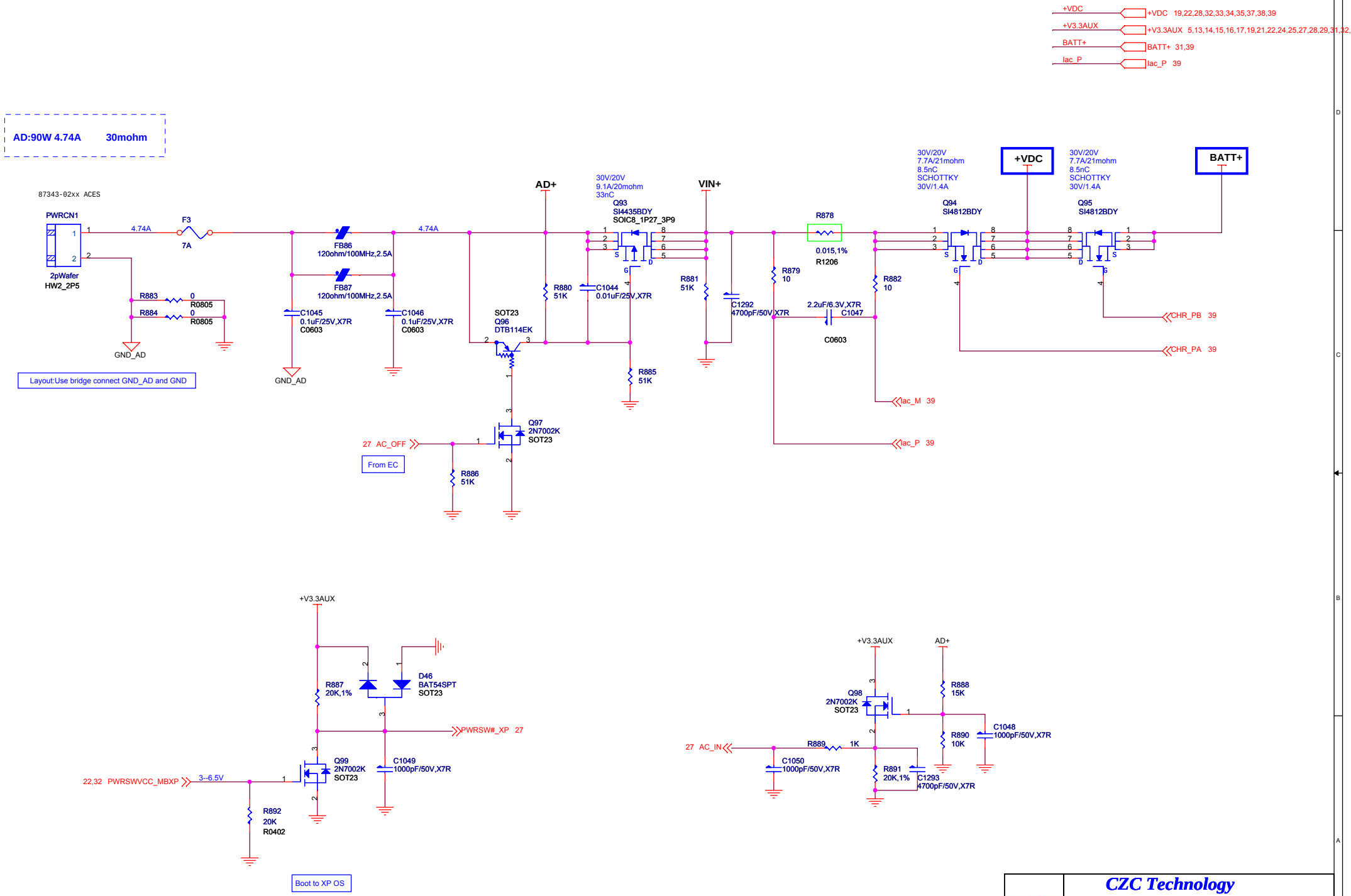
+VDC 19,22,28,32,33,34,35,37,38,39
+V3.3AUX 5,13,14,15,16,17,19,21,22,24,25,27,28,29,31,32,34
BATT+ 31,39
Iac_P 39
AD:90W 4.74A 30mohm
87343-02xx ACES
PWRCN1
2pWafer
HW2_2P5
4.74A
F3
7A
R883 0 R0805
R884 0 R0805
GND_AD
Layout:Use bridge connect GND_AD and GND
FB86
120ohm/100MHz,2.5A
FB87
120ohm/100MHz,2.5A
C1045
0.1uF/25V,X7R
C0603
C1046
0.1uF/25V,X7R
C0603
AD+
SOT23
Q96
DTB114EK
R880
51K
30V/20V
9.1A/20mohm
33nC
Q93
SI4435BDY
SOIC8_1P27_3P9
C1044
0.01uF/25V,X7R
R885
51K
VIN+
R881
51K
C1292
4700pF/50V,X7R
R878
0.015,1%
R1206
R879
10
2.2uF/6.3V,X7R
C1047
C0603
R882
10
30V/20V
7.7A/21mohm
8.5nC
SCHOTTKY
30V/1.4A
Q94
SI4812BDY
+VDC
30V/20V
7.7A/21mohm
8.5nC
SCHOTTKY
30V/1.4A
Q95
SI4812BDY
BATT+
CHR_PB 39
CHR_PA 39
Iac_M 39
Iac_P 39
Q97
2N7002K
SOT23
27 AC_OFF
From EC
R886
51K
+V3.3AUX
R887
20K,1%
D46
BAT54SPT
SOT23
PWRSW#_XP 27
Q99
2N7002K
SOT23
C1049
1000pF/50V,X7R
22,32 PWRSWVCC_MBXP
3~6.5V
R892
20K
R0402
Boot to XP OS
+V3.3AUX
AD+
Q98
2N7002K
SOT23
R888
15K
R890
10K
C1048
1000pF/50V,X7R
27 AC_IN
R889
1K
C1050
1000pF/50V,X7R
R891
20K,1%
C1293
4700pF/50V,X7R
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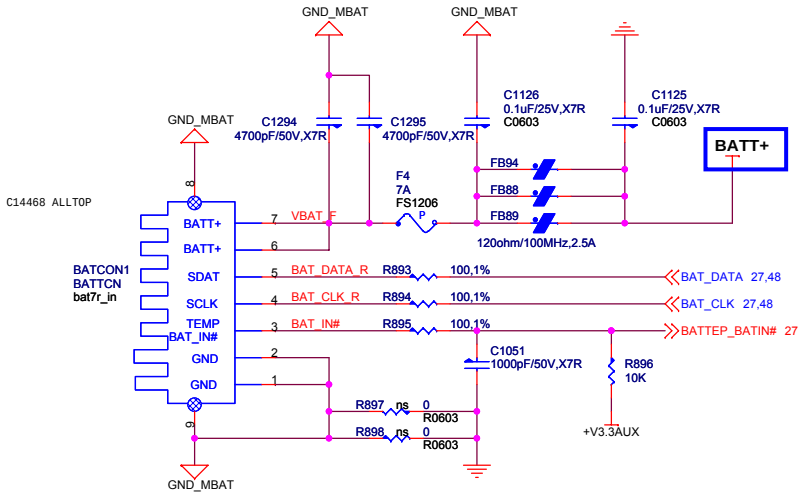
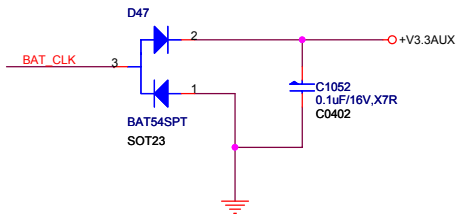
BATT+ — BATT+ 30,39

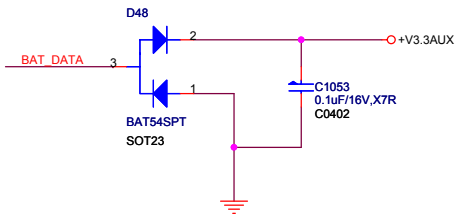
+V3.3AUX — +V3.3AUX 5,13,14,15,16,17,19,21,22,24,25,27,28,29,30,32,34



Use bridge connect GND_MBAT and GND

BATTEP_BATIN#	
0.5-2.5V	Battery OK
<0.5V or >2.5V	Battery Fail





CZC Technology		
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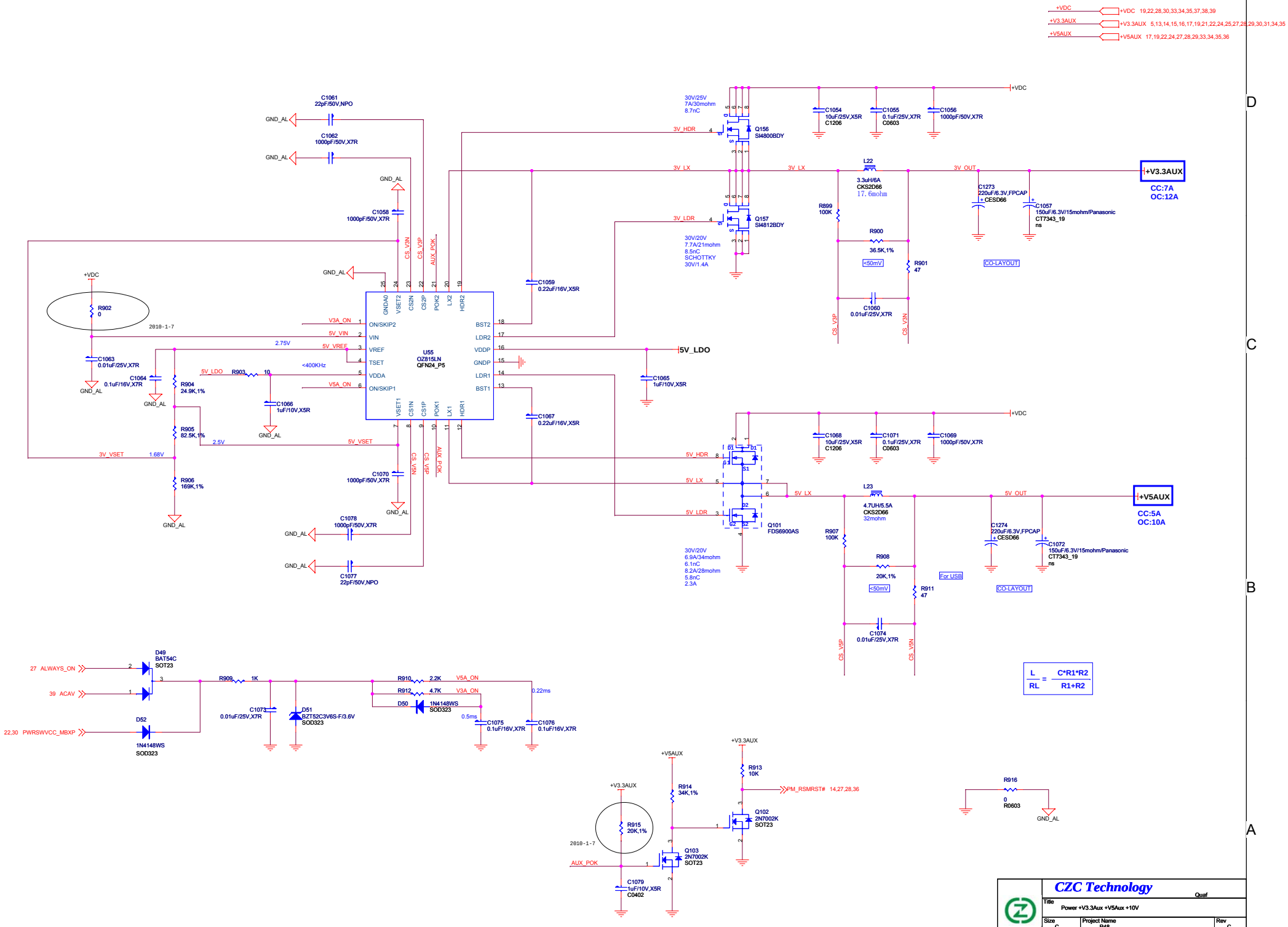
+VDC 19,22,28,30,33,34,35,37,38,39
+V3.3AUX 5,13,14,15,16,17,19,21,22,24,25,27,28,29,30,31,34,35
+V5AUX 17,19,22,24,27,28,29,33,34,35,36
U55
OZ815LN
QFN24_P5
ON/SKIP2
VIN
VREF
TSET
VDDA
ON/SKIP1
BST2
LDR2
VDDP
GNDP
LDR1
BST1
GND/A0
VSET2
CS2N
CS2P
POK2
LX2
HDR2
VSET1
CS1N
CS1P
POK1
LX1
HDR1
Q156
SI4800BDY
Q157
SI4812BDY
Q101
FDS6900AS
L22
3.3uH/6A
CKS2D66
17.6mohm
L23
4.7UH/5.5A
CKS2D66
32mohm
+V3.3AUX
CC:7A
OC:12A
+V5AUX
CC:5A
OC:10A
5V_LDO
CO-LAYOUT
For USB
L / RL = C*R1*R2 / R1+R2
D49
BAT54C
SOT23
D52
1N4148WS
SOD323
D51
BZT52C3V6S-F/3.6V
SOD323
D50
1N4148WS
SOD323
Q102
2N7002K
SOT23
Q103
2N7002K
SOT23
PM_RSMRST# 14,27,28,36
27 ALWAYS_ON
39 ACAV
22,30 PWRSWVCC_MBXP
CZC Technology
Title
Power +V3.3Aux +V5Aux +10V
Size C
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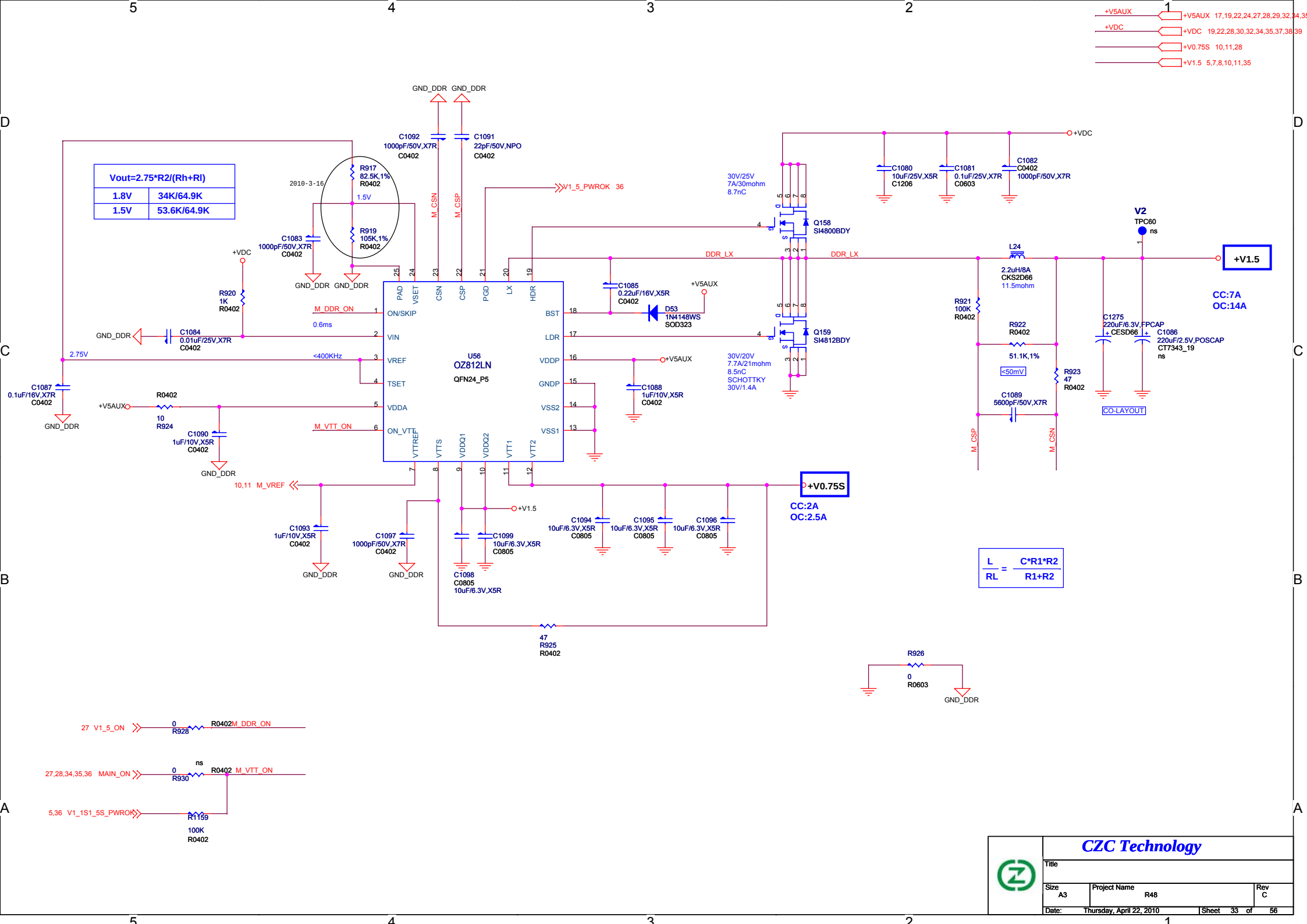
+V5AUX 17,19,22,24,27,28,29,32,34,35
+VDC 19,22,28,30,32,34,35,37,38,39
+V0.75S 10,11,28
+V1.5 5,7,8,10,11,35
Vout=2.75*R2/(Rh+Rl)
1.8V 34K/64.9K
1.5V 53.6K/64.9K
2010-3-16
R917 82.5K,1% R0402
R919 105K,1% R0402
1.5V
C1083 1000pF/50V,X7R C0402
C1092 1000pF/50V,X7R C0402
C1091 22pF/50V,NPO C0402
GND_DDR
M_CSN
M_CSP
V1_5_PWROK 36
R920 1K R0402
C1084 0.01uF/25V,X7R C0402
M_DDR_ON
0.6ms
2.75V
<400KHz
C1087 0.1uF/16V,X7R C0402
+V5AUX
R0402 10 R924
C1090 1uF/10V,X5R C0402
M_VTT_ON
10,11 M_VREF
C1093 1uF/10V,X5R C0402
C1097 1000pF/50V,X7R C0402
C1098 C0805 10uF/6.3V,X5R
C1099 10uF/6.3V,X5R C0805
+V1.5
C1094 10uF/6.3V,X5R C0805
C1095 10uF/6.3V,X5R C0805
C1096 10uF/6.3V,X5R C0805
47 R925 R0402
U56
OZ812LN
QFN24_P5
PAD VSET CSN CSP PGD LX HDR
ON/SKIP VIN VREF TSET VDDA ON_VTT
BST LDR VDDP GNDP VSS2 VSS1
VTTREF VTTS VDDQ1 VDDQ2 VTT1 VTT2
C1085 0.22uF/16V,X5R C0402
D53 1N4148WS SOD323
C1088 1uF/10V,X5R C0402
30V/25V 7A/30mohm 8.7nC
Q158 SI4800BDY
DDR_LX
30V/20V 7.7A/21mohm 8.5nC SCHOTTKY 30V/1.4A
Q159 SI4812BDY
+VDC
C1080 10uF/25V,X5R C1206
C1081 0.1uF/25V,X7R C0603
C1082 C0402 1000pF/50V,X7R
L24 2.2uH/8A CKS2D66 11.5mohm
R921 100K R0402
R922 R0402 51.1K,1%
<50mV
C1089 5600pF/50V,X7R
R923 47 R0402
C1275 220uF/6.3V,FPCAP CESD66
C1086 220uF/2.5V,POSCAP CT7343_19 ns
CO-LAYOUT
V2 TPC60 ns
+V1.5
CC:7A
OC:14A
+V0.75S
CC:2A
OC:2.5A
L/RL = C*R1*R2/(R1+R2)
R926 0 R0603
27 V1_5_ON
0 R928 R0402 M_DDR_ON
27,28,34,35,36 MAIN_ON
0 R930 ns R0402 M_VTT_ON
5,36 V1_1S1_5S_PWROK
R1159 100K R0402
CZC Technology
Title
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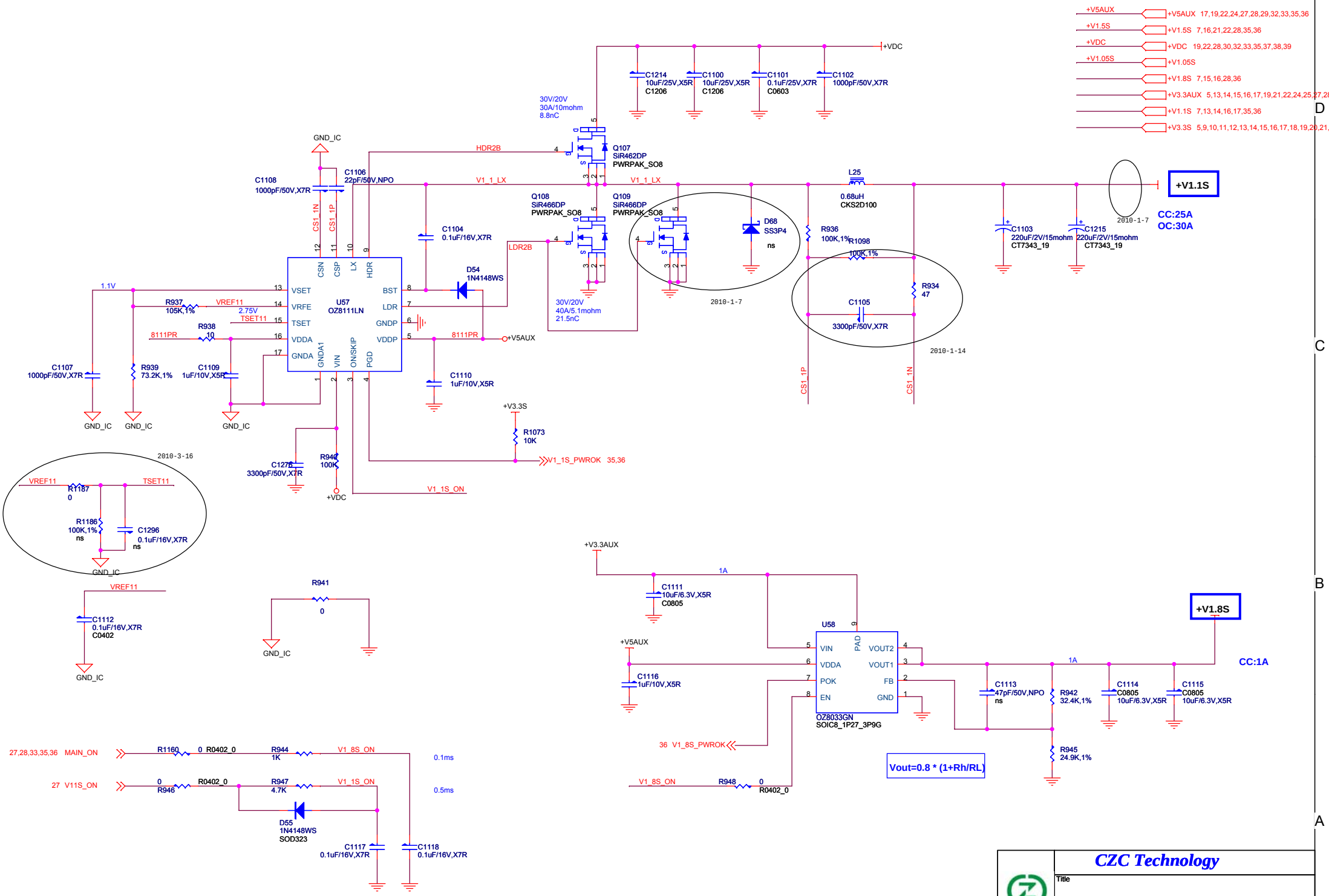
+V5AUX 17,19,22,24,27,28,29,32,33,35,36
+V1.5S 7,16,21,22,28,35,36
+VDC 19,22,28,30,32,33,35,37,38,39
+V1.05S
+V1.8S 7,15,16,28,36
+V3.3AUX 5,13,14,15,16,17,19,21,22,24,25,27,28
+V1.1S 7,13,14,16,17,35,36
+V3.3S 5,9,10,11,12,13,14,15,16,17,18,19,20,21,
+VDC
C1214 10uF/25V,X5R C1206
C1100 10uF/25V,X5R C1206
C1101 0.1uF/25V,X7R C0603
C1102 1000pF/50V,X7R
30V/20V 30A/10mohm 8.8nC
Q107 SiR462DP PWRPAK_SO8
HDR2B
GND_IC
C1108 1000pF/50V,X7R
C1106 22pF/50V,NPO
V1_1_LX
Q108 SiR466DP PWRPAK_SO8
Q109 SiR466DP PWRPAK_SO8
L25 0.68uH CKS2D100
+V1.1S
CC:25A
OC:30A
2010-1-7
C1104 0.1uF/16V,X7R
LDR2B
D68 SS3P4 ns
R936 100K,1%
R1098 100K,1%
C1103 220uF/2V/15mohm CT7343_19
C1215 220uF/2V/15mohm CT7343_19
CS1_1N
CS1_1P
D54 1N4148WS
30V/20V 40A/5.1mohm 21.5nC
R934 47
C1105 3300pF/50V,X7R
2010-1-14
1.1V
R937 105K,1%
VREF11
2.75V
TSET11
R938 10
8111PR
U57 OZ8111LN
VSET
VRFE
TSET
VDDA
GNDA
BST
LDR
GNDP
VDDP
GNDA1
VIN
ON/SKIP
PGD
CSN
CSP
LX
HDR
+V5AUX
C1107 1000pF/50V,X7R
R939 73.2K,1%
C1109 1uF/10V,X5R
C1110 1uF/10V,X5R
+V3.3S
R1073 10K
V1_1S_PWROK 35,36
C1276 3300pF/50V,X7R
R940 100K
+VDC
V1_1S_ON
2010-3-16
R1187 0
R1186 100K,1% ns
C1296 0.1uF/16V,X7R ns
C1112 0.1uF/16V,X7R C0402
R941 0
+V3.3AUX
1A
C1111 10uF/6.3V,X5R C0805
U58
VIN
VDDA
POK
EN
PAD
VOUT2
VOUT1
FB
GND
OZ8033GN SOIC8_1P27_3P9G
C1116 1uF/10V,X5R
+V1.8S
CC:1A
C1113 47pF/50V,NPO ns
R942 32.4K,1%
C1114 C0805 10uF/6.3V,X5R
C1115 C0805 10uF/6.3V,X5R
R945 24.9K,1%
36 V1_8S_PWROK
V1_8S_ON
R948 0 R0402_0
Vout=0.8 * (1+Rh/RL)
27,28,33,35,36 MAIN_ON
R1160 0 R0402_0
R944 1K
V1_8S_ON
0.1ms
27 V11S_ON
R946 0 R0402_0
R947 4.7K
V1_1S_ON
0.5ms
D55 1N4148WS SOD323
C1117 0.1uF/16V,X7R
C1118 0.1uF/16V,X7R
CZC Technology
Title
Size A3
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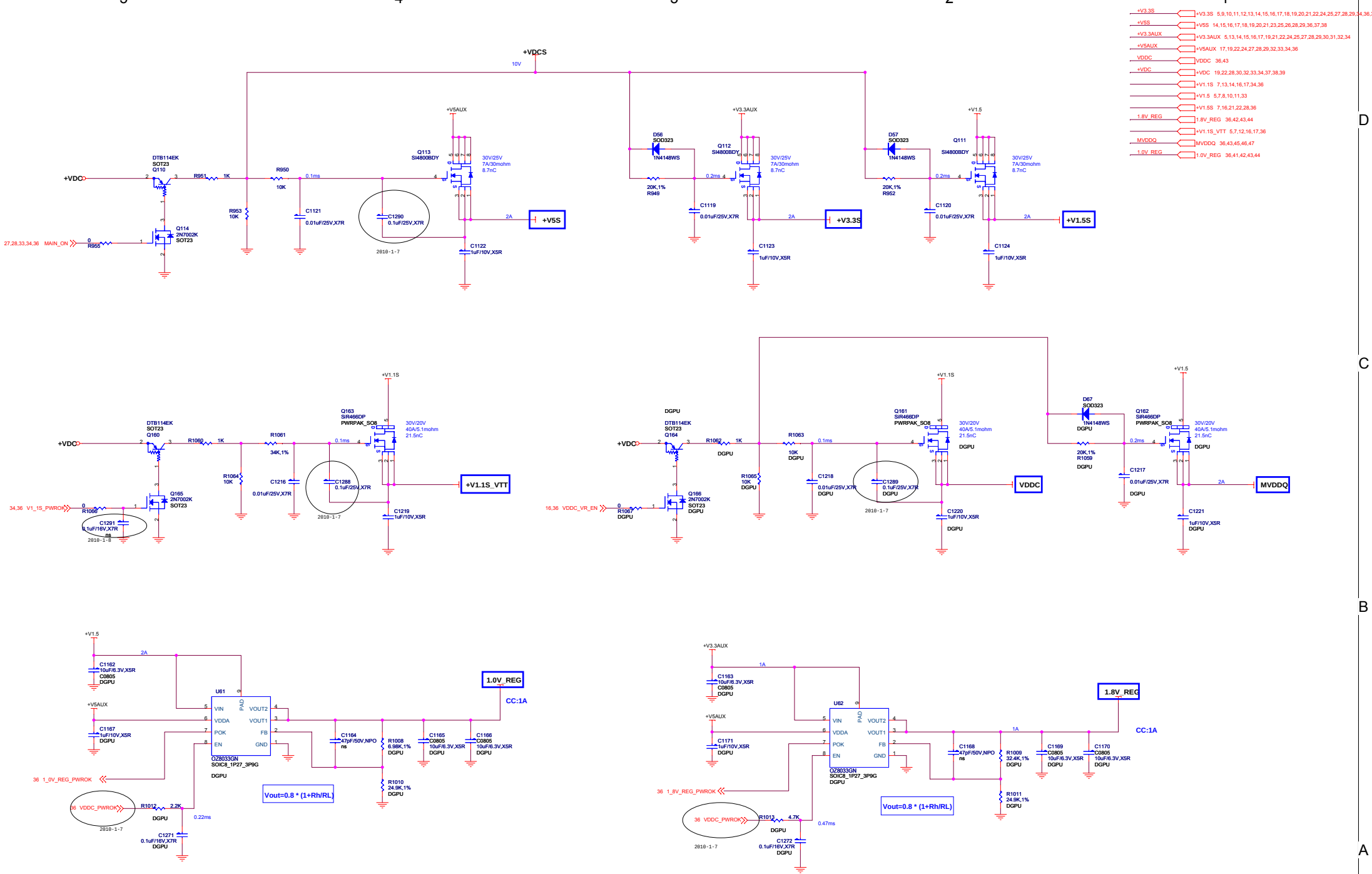

CZC Technology	
Title	
Size A2	Project Name R48
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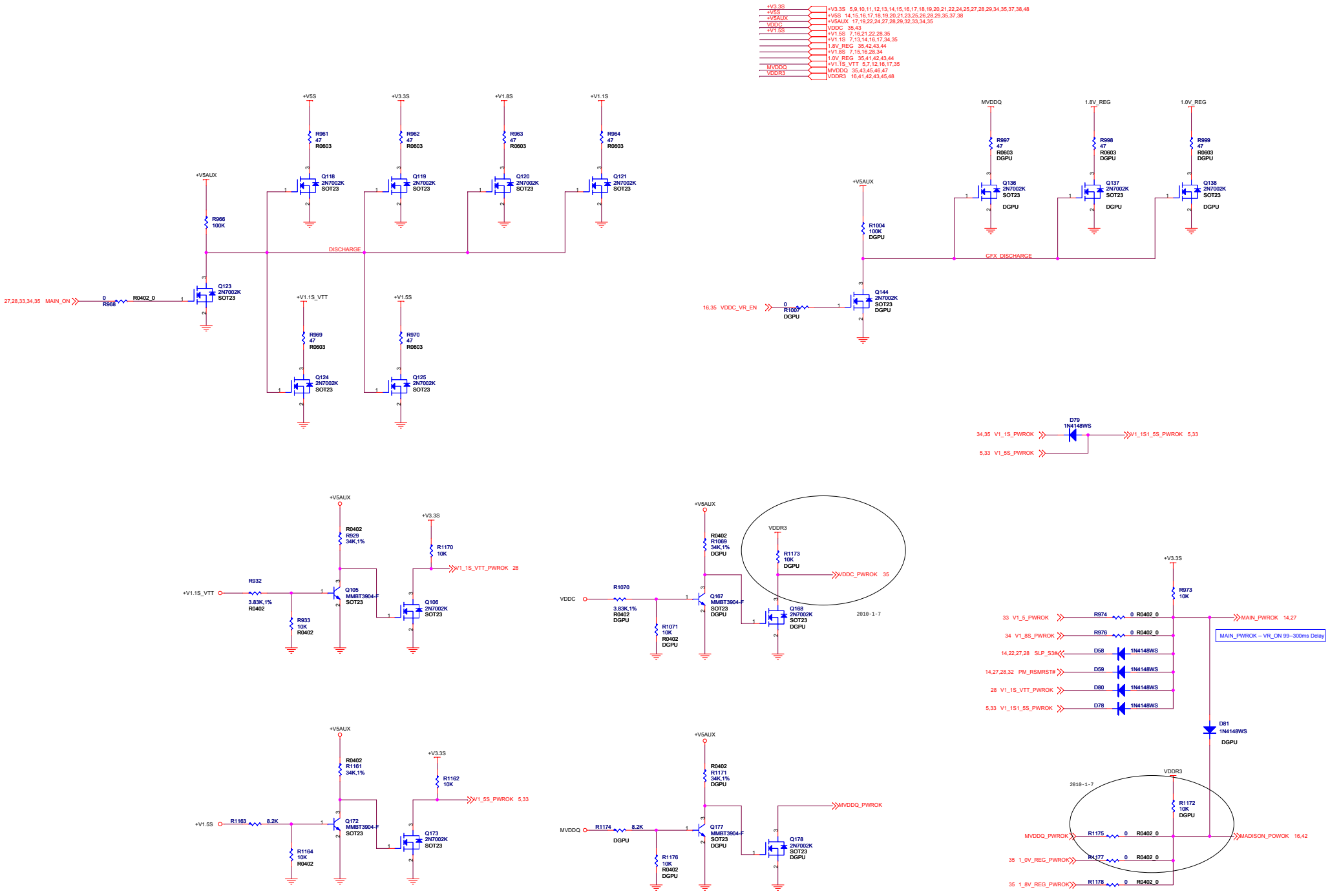
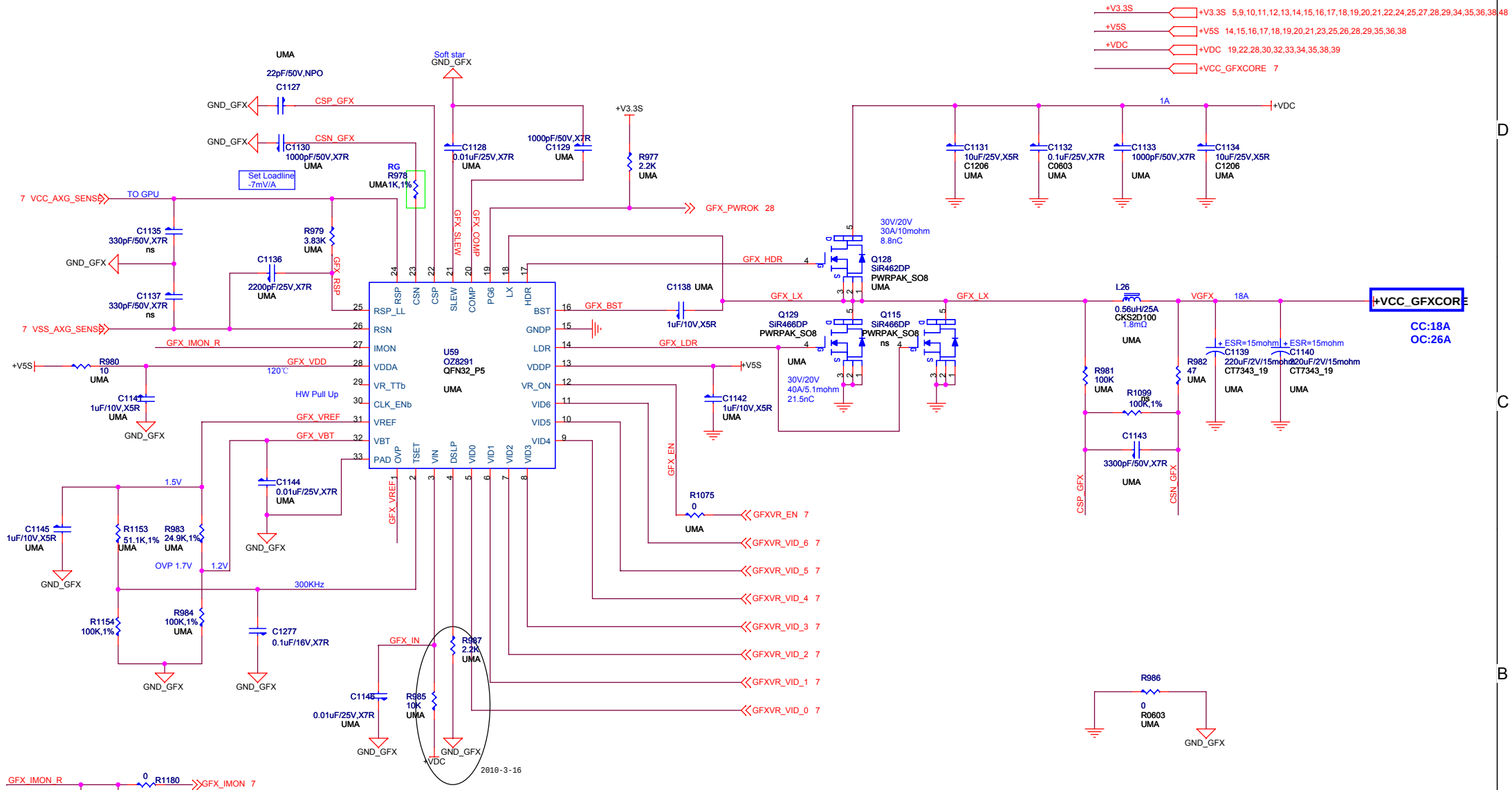


CZC Technology		
Title		
Size A2	Project Name R48	Rev C
Date: Thursday, April 22, 2010	Sheet 36 of 56	



GFX CORE Debug

VID6	VID5	VID4	VID3	VID2	VID1	VID0	Vout
0	0	1	1	0	0	0	1.2000V
0	1	1	0	0	0	0	0.9000V

CZC Technology

Title		
Size A3	Project Name R48	Rev C
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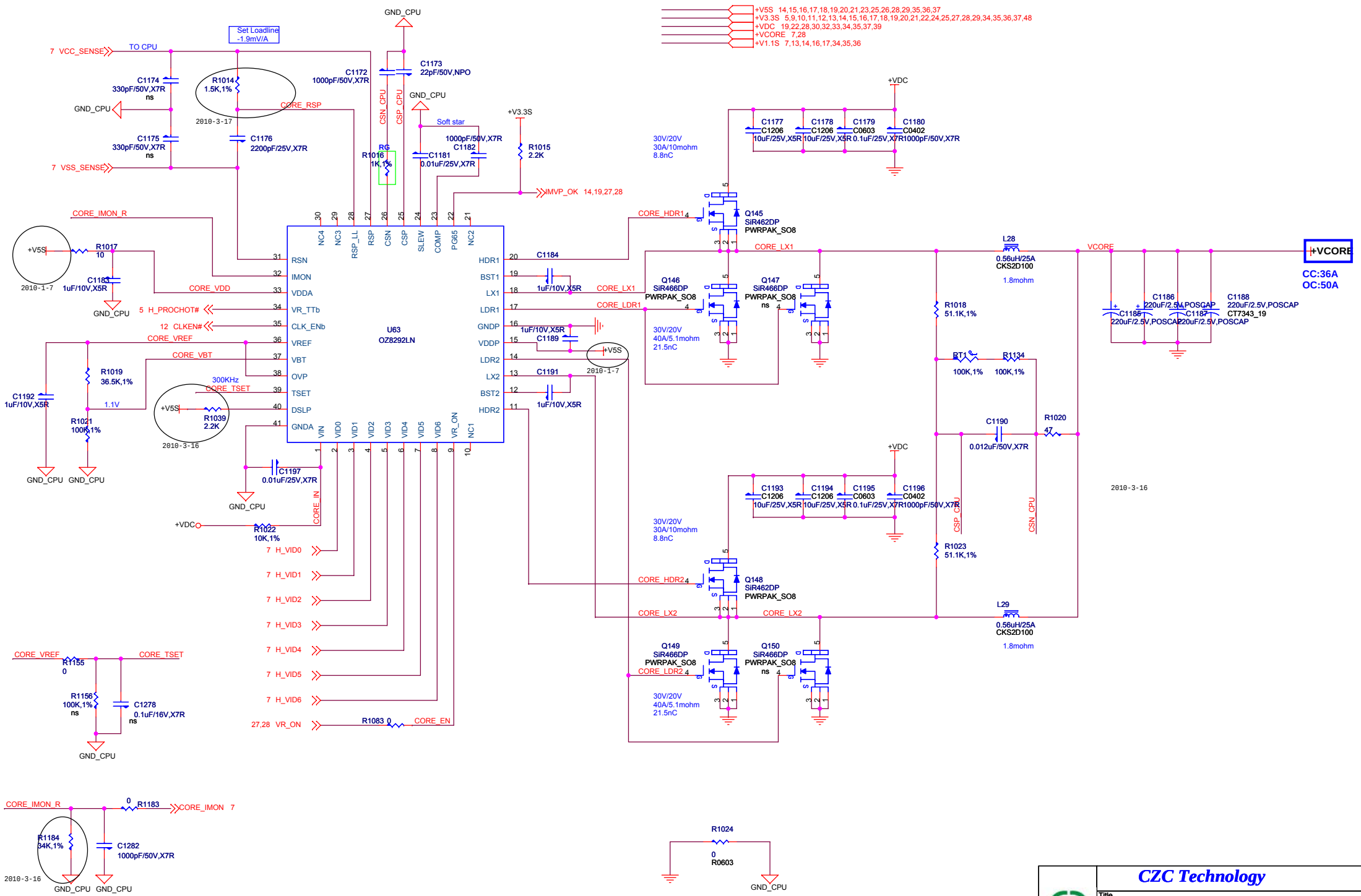
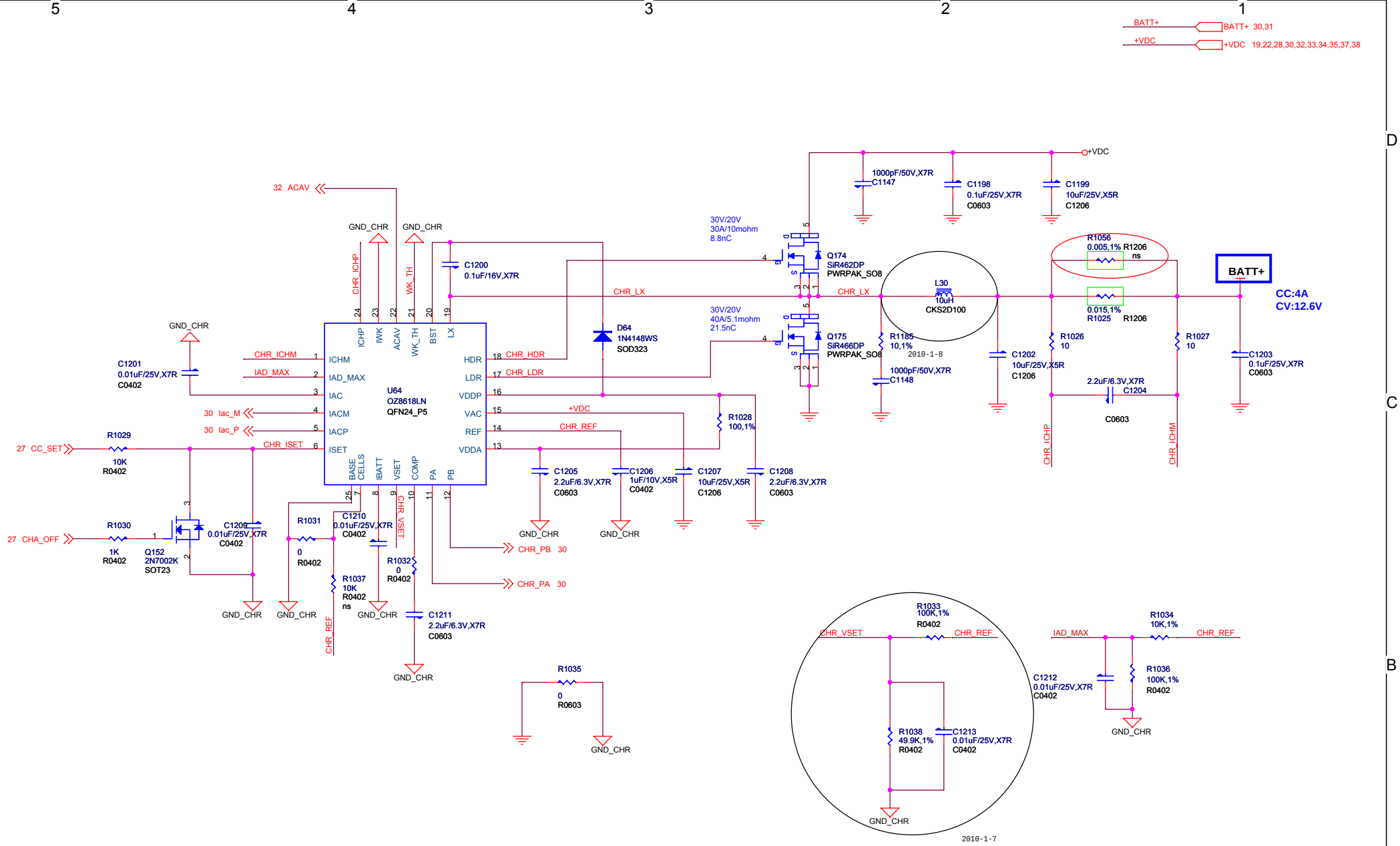

+V5S 14,15,16,17,18,19,20,21,23,25,26,28,29,35,36,37
+V3.3S 5,9,10,11,12,13,14,15,16,17,18,19,20,21,22,24,25,27,28,29,34,35,36,37,48
+VDC 19,22,28,30,32,33,34,35,37,39
+VCORE 7,28
+V1.1S 7,13,14,16,17,34,35,36
GND_CPU
Set Loadline
-1.9mV/A
7 VCC_SENSE
TO CPU
C1174
330pF/50V,X7R
ns
R1014
1.5K,1%
2010-3-17
C1172
1000pF/50V,X7R
C1173
22pF/50V,NPO
CSN_CPU
CSP_CPU
CORE_RSP
C1175
330pF/50V,X7R
ns
C1176
2200pF/25V,X7R
7 VSS_SENSE
R1016
1K,1%
RG
Soft star
C1181
0.01uF/25V,X7R
1000pF/50V,X7R
C1182
+V3.3S
R1015
2.2K
IMVP_OK 14,19,27,28
CORE_IMON_R
+V5S
R1017
10
2010-1-7
C1183
1uF/10V,X5R
CORE_VDD
5 H_PROCHOT#
12 CLKEN#
CORE_VREF
CORE_VBT
R1019
36.5K,1%
C1192
1uF/10V,X5R
1.1V
R1021
100K,1%
300KHz
CORE_TSET
R1039
2.2K
2010-3-16
U63
OZ8292LN
NC4 NC3 RSP_LL RSP CSN CSP SLEW COMP PG65 NC2
RSN IMON VDDA VR_TTb CLK_ENb VREF VBT OVP TSET DSLP GNDA
HDR1 BST1 LX1 LDR1 GNDP VDDP LDR2 LX2 BST2 HDR2
VIN VID0 VID1 VID2 VID3 VID4 VID5 VID6 VR_ON NC1
C1184
1uF/10V,X5R
CORE_LX1
CORE_LDR1
C1189
C1191
1uF/10V,X5R
C1197
0.01uF/25V,X7R
CORE_IN
+VDC
R1022
10K,1%
7 H_VID0
7 H_VID1
7 H_VID2
7 H_VID3
7 H_VID4
7 H_VID5
7 H_VID6
27,28 VR_ON
R1083 0
CORE_EN
CORE_HDR1
Q145
SiR462DP
PWRPAK_SO8
Q146
SiR466DP
PWRPAK_SO8
Q147
SiR466DP
PWRPAK_SO8
ns
30V/20V
40A/5.1mohm
21.5nC
30V/20V
30A/10mohm
8.8nC
C1177
C1206
10uF/25V,X5R
C1178
C1206
10uF/25V,X5R
C1179
C0603
0.1uF/25V,X7R
C1180
C0402
1000pF/50V,X7R
L28
0.56uH/25A
CKS2D100
1.8mohm
VCORE
+VCORE
CC:36A
OC:50A
C1185
220uF/2.5V,POSCAP
C1186
220uF/2.5V,POSCAP
C1187
220uF/2.5V,POSCAP
C1188
220uF/2.5V,POSCAP
CT7343_19
R1018
51.1K,1%
RT1
100K,1%
R1134
100K,1%
C1190
0.012uF/50V,X7R
R1020
47
2010-3-16
C1193
C1206
10uF/25V,X5R
C1194
C1206
10uF/25V,X5R
C1195
C0603
0.1uF/25V,X7R
C1196
C0402
1000pF/50V,X7R
R1023
51.1K,1%
CORE_HDR2
Q148
SiR462DP
PWRPAK_SO8
CORE_LX2
L29
0.56uH/25A
CKS2D100
1.8mohm
Q149
SiR466DP
PWRPAK_SO8
Q150
SiR466DP
PWRPAK_SO8
ns
CORE_LDR2
CORE_VREF
R1155
0
CORE_TSET
R1156
100K,1%
ns
C1278
0.1uF/16V,X7R
ns
CORE_IMON_R
0
R1183
CORE_IMON 7
R1184
34K,1%
C1282
1000pF/50V,X7R
2010-3-16
R1024
0
R0603
CZC Technology
Title
Size
A3
Project Name
R48
Rev
C
Date:
Thursday, April 22, 2010
Sheet 38 of 56



CC_SET	Charge Current	SystemState	Cells
3.0V	4.17A	S3,S4,S5	6Cells
2.0V	2.78A	S0	6Cells
1.5V	2.08A	S0,S3,S4,S5	3Cells
0.375V	521mA	PreCharge	3Cells/6Cells
<0.15V	=CHA_OFF		3Cells/6Cells

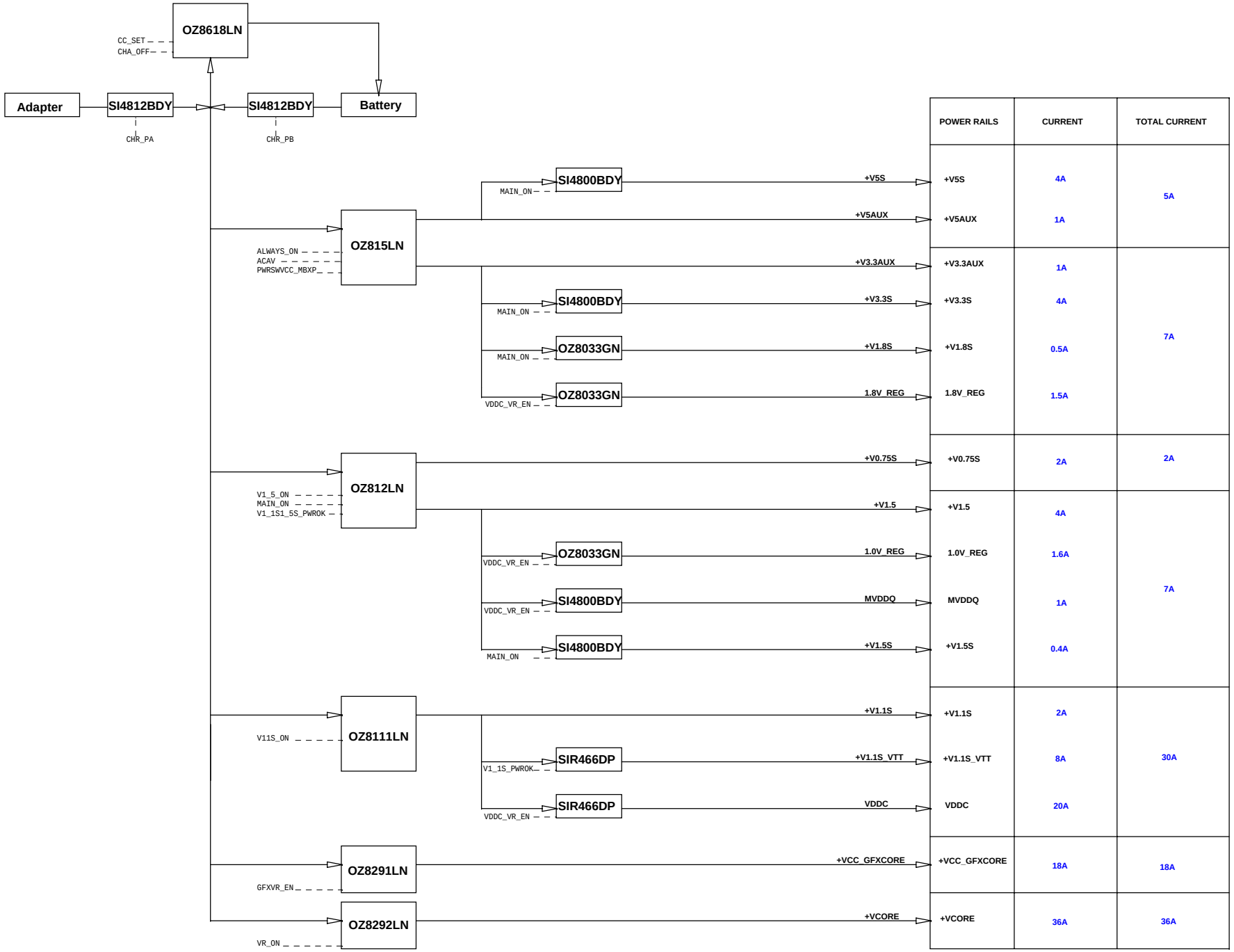
State	CELLS
Hi_Z	2
LOW	3

CZC Technology

Title

Size	Project Name	Rev
A3	R48	C

Date: Thursday, April 22, 2010 Sheet 39 of 56



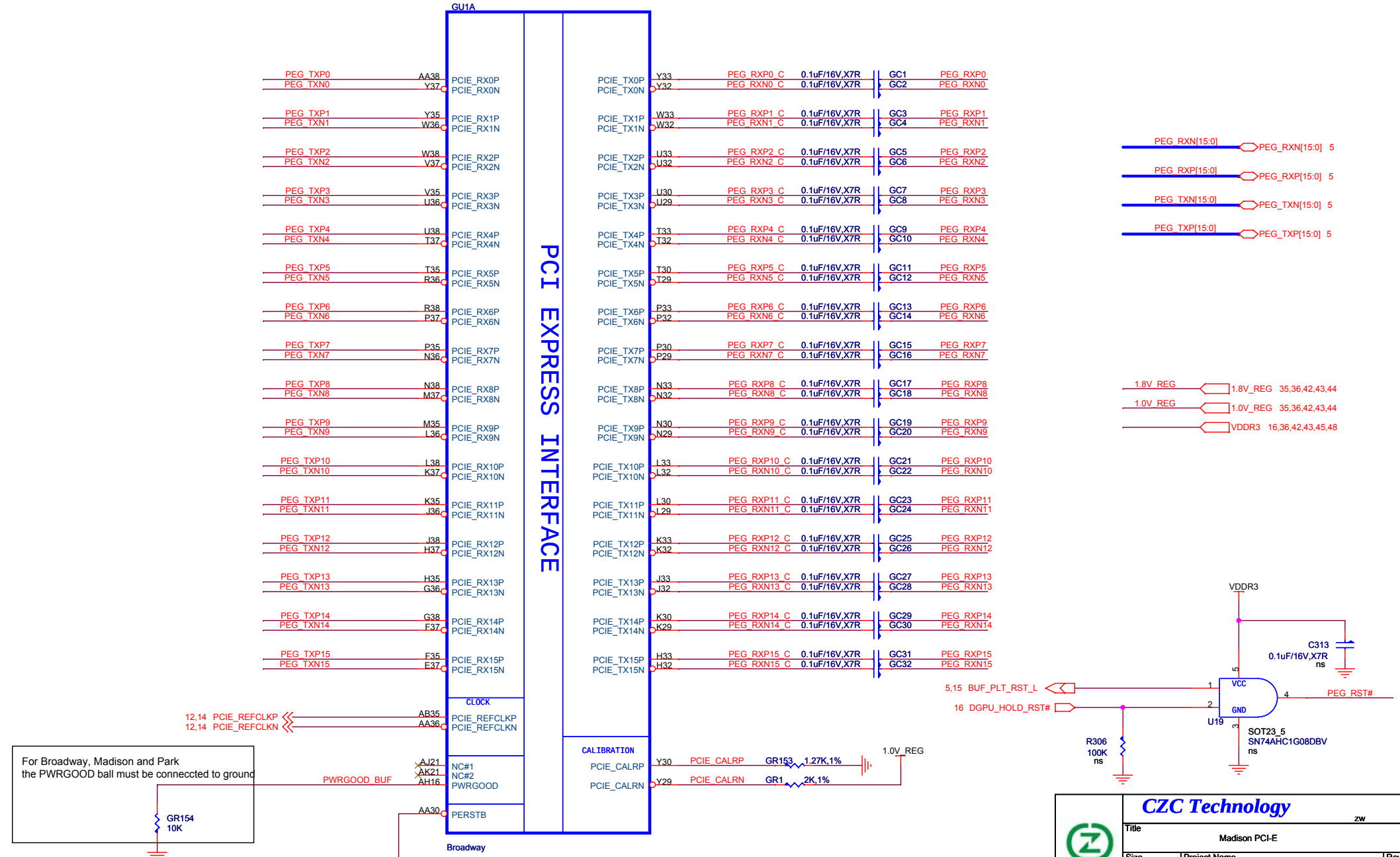
POWER RAILS	CURRENT	TOTAL CURRENT
+V5S	4A	5A
+V5AUX	1A	
+V3.3AUX	1A	7A
+V3.3S	4A	
+V1.8S	0.5A	
1.8V_REG	1.5A	
+V0.75S	2A	2A
+V1.5	4A	7A
1.0V_REG	1.6A	
MVDDQ	1A	
+V1.5S	0.4A	
+V1.1S	2A	30A
+V1.1S_VTT	8A	
VDDC	20A	
+VCC_GFXCORE	18A	18A
+VCORE	36A	36A

CZC Technology

Title

Size	Project Name	Rev
A3	R48	C

Date: Thursday, April 22, 2010 Sheet 40 of 56



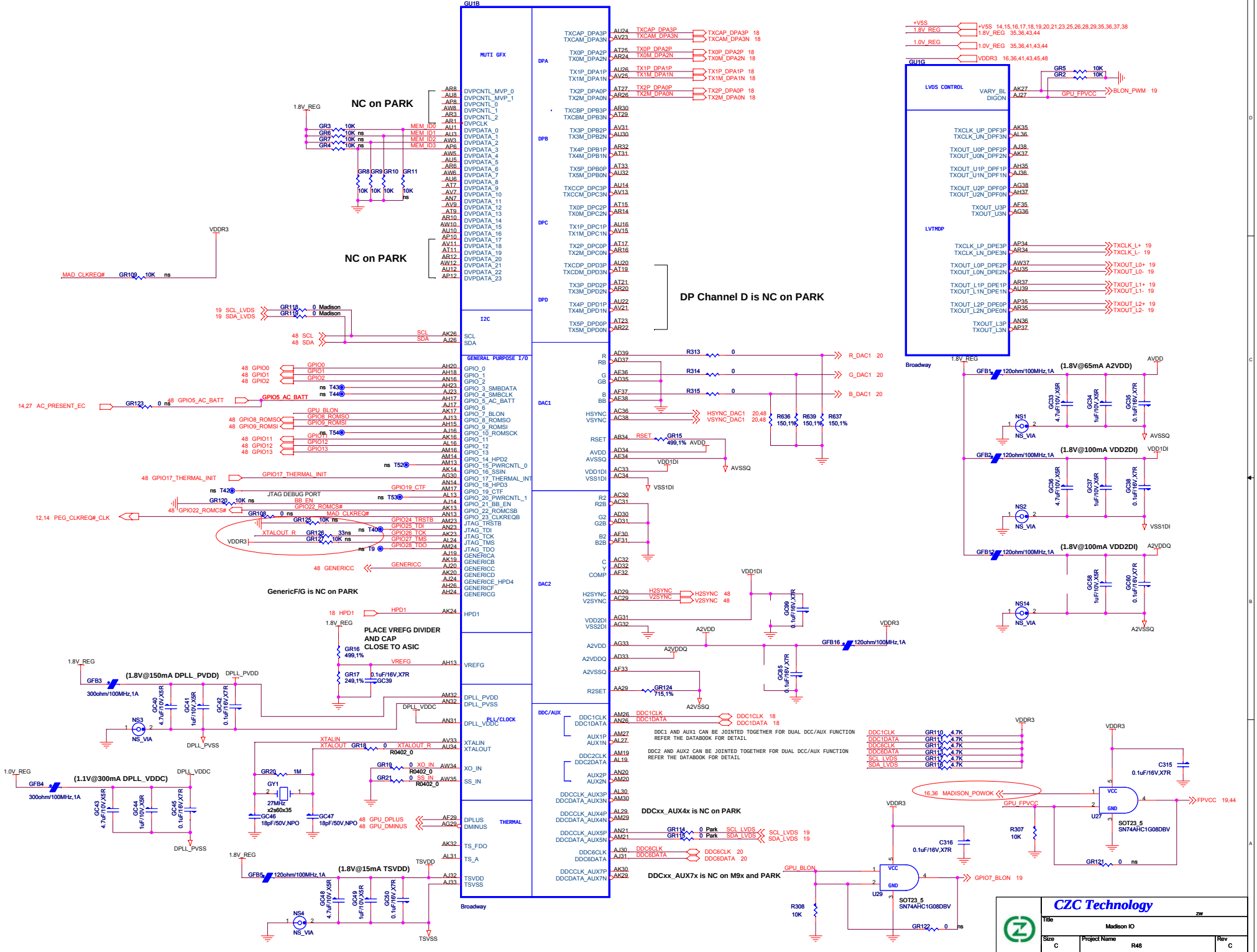
CZC Technology

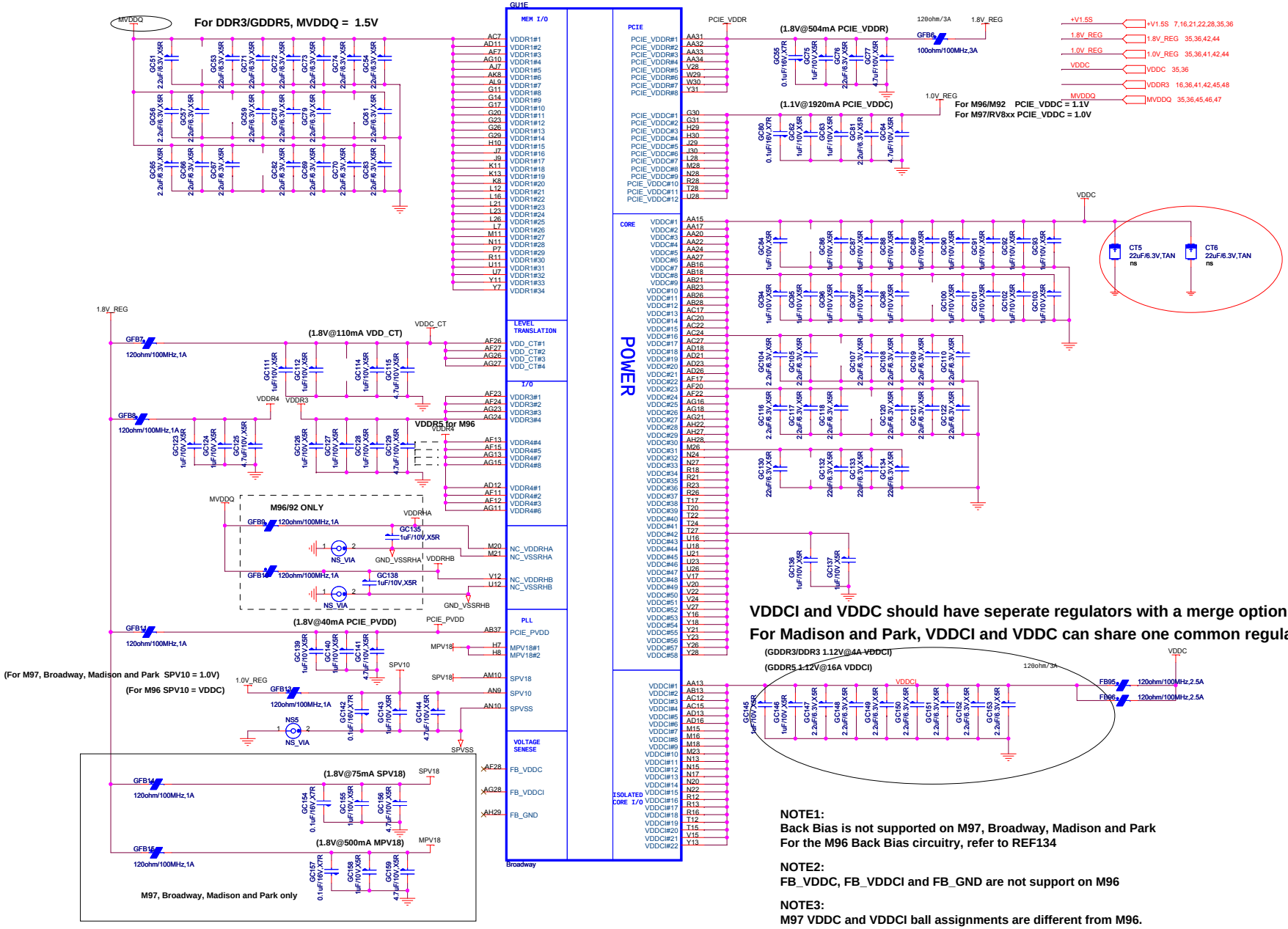
zw

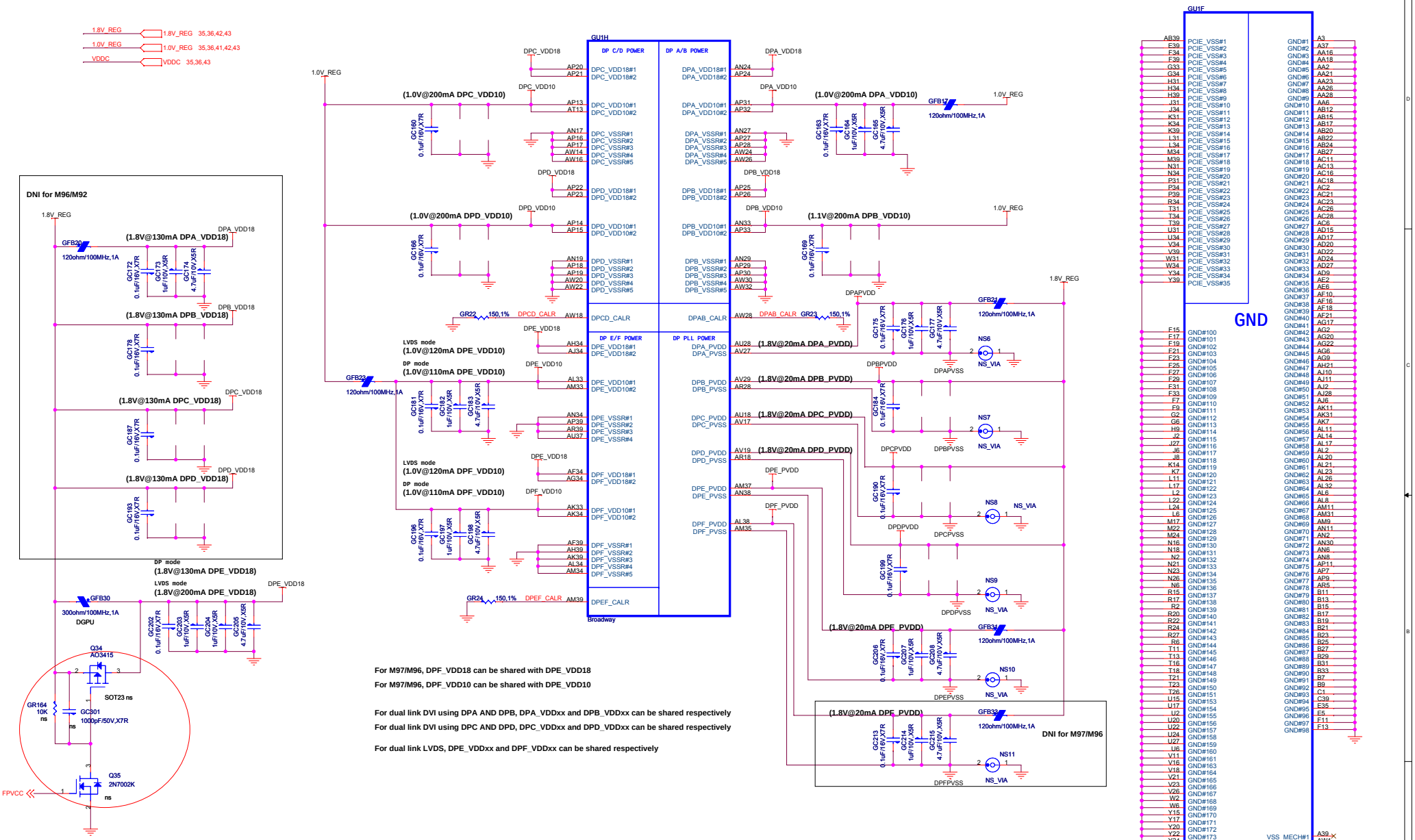
Title: Madison PCI-E

Size: B | Project Name: R48 | Rev: C

Date: Thursday, April 22, 2010 | Sheet 41 of 56

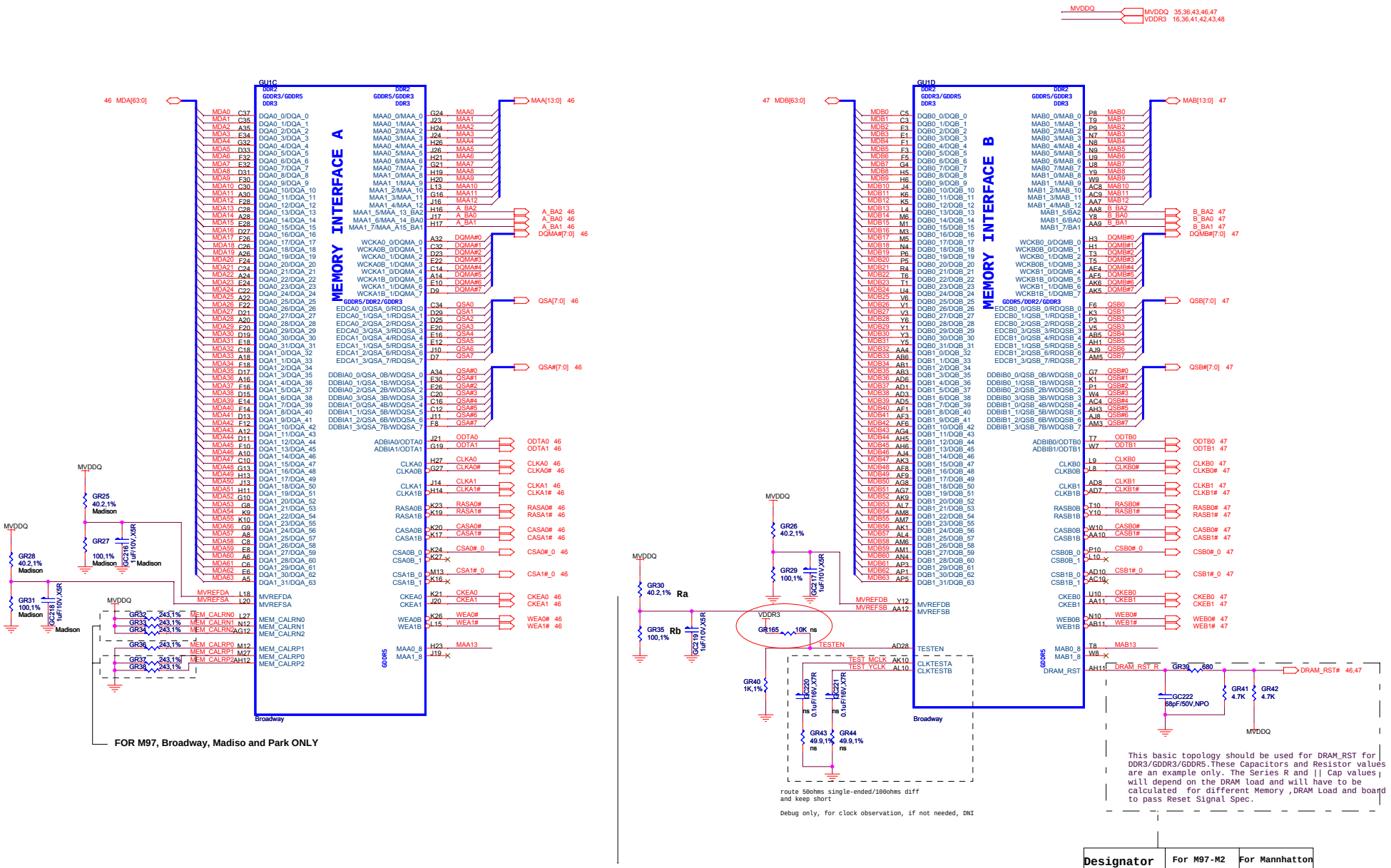

GU1B
MUTI GFX
NC on PARK
NC on PARK
DP Channel D is NC on PARK
GenericF/G is NC on PARK
PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC
(1.8V@150mA DPLL_PVDD)
(1.1V@300mA DPLL_VDDC)
(1.8V@15mA TSVDD)
DDCxx_AUX4x is NC on PARK
DDCxx_AUX7x is NC on M9x and PARK
DDC1 AND AUX1 CAN BE JOINTED TOGETHER FOR DUAL DCC/AUX FUNCTION
REFER THE DATABOOK FOR DETAIL
DDC2 AND AUX2 CAN BE JOINTED TOGETHER FOR DUAL DCC/AUX FUNCTION
REFER THE DATABOOK FOR DETAIL
Broadway
GU1G
LVDS CONTROL
LVTMDP
(1.8V@65mA A2VDD)
(1.8V@100mA VDD2DI)
(1.8V@100mA VDD2DI)
SOT23_5
SN74AHC1G08DBV
CZC Technology
Title
Madison IO
Size
C
Project Name
R48
Rev
C
Date:
Thursday, April 22, 2010
Sheet 42 of 56


For DDR3/GDDR5, MVDDQ = 1.5V
GU1E
MEM I/O
PCIE
LEVEL TRANSLATION
I/O
POWER
PLL
VOLTAGE SENESE
ISOLATED CORE I/O
Broadway
(1.8V@504mA PCIE_VDDR)
(1.1V@1920mA PCIE_VDDC)
For M96/M92 PCIE_VDDC = 1.1V
For M97/RV8xx PCIE_VDDC = 1.0V
(1.8V@110mA VDD_CT)
VDDR5 for M96
M96/92 ONLY
(1.8V@40mA PCIE_PVDD)
(For M97, Broadway, Madison and Park SPV10 = 1.0V)
(For M96 SPV10 = VDDC)
(1.8V@75mA SPV18)
(1.8V@500mA MPV18)
M97, Broadway, Madison and Park only
CT5 22uF/6.3V,TANns
CT6 22uF/6.3V,TANns
(GDDR3/DDR3 1.12V@4A VDDCI)
(GDDR5 1.12V@16A VDDCI)
VDDCI and VDDC should have seperate regulators with a merge option on PCB
For Madison and Park, VDDCI and VDDC can share one common regulator
NOTE1:
Back Bias is not supported on M97, Broadway, Madison and Park
For the M96 Back Bias circuitry, refer to REF134
NOTE2:
FB_VDDC, FB_VDDCI and FB_GND are not support on M96
NOTE3:
M97 VDDC and VDDCI ball assignments are different from M96.
If M96 is populated on this design, VDDC and VDDCI will be shorted on the substrate.
NOTE4:
For M2 design compatibility, refer to the document AN_M96_Ax and AN_M97_Ax
M97, Broadway, Madison and Park only
M96 do not support core vsense feature
VCORE_SEN/RTN and VDDCI_SEN/RTN route as differetial pair
CZC Technology
Title
Madison Power
Size
C
Project Name
R48
Rev
C
Date: Thursday, April 22, 2010
Sheet 43 of 56



CZC Technology

Title	Madison DP Power		zw
Size C	Project Name R48		Rev C
Date: Thursday, April 22, 2010		Sheet 44 of 56	



DDR3/GDDR3 Memory Stuff Option

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

Designator	For M97-M2	For Mannhatton
R_MEM_1	10K	10K
R_MEM_2	0R/Short	680R
R_MEM_3	DNI	DNI
C_MEM	2.2nF	68pF

CZC Technology

zw

Title: Madison Memory

Size: C | Project Name: R48 | Rev: C

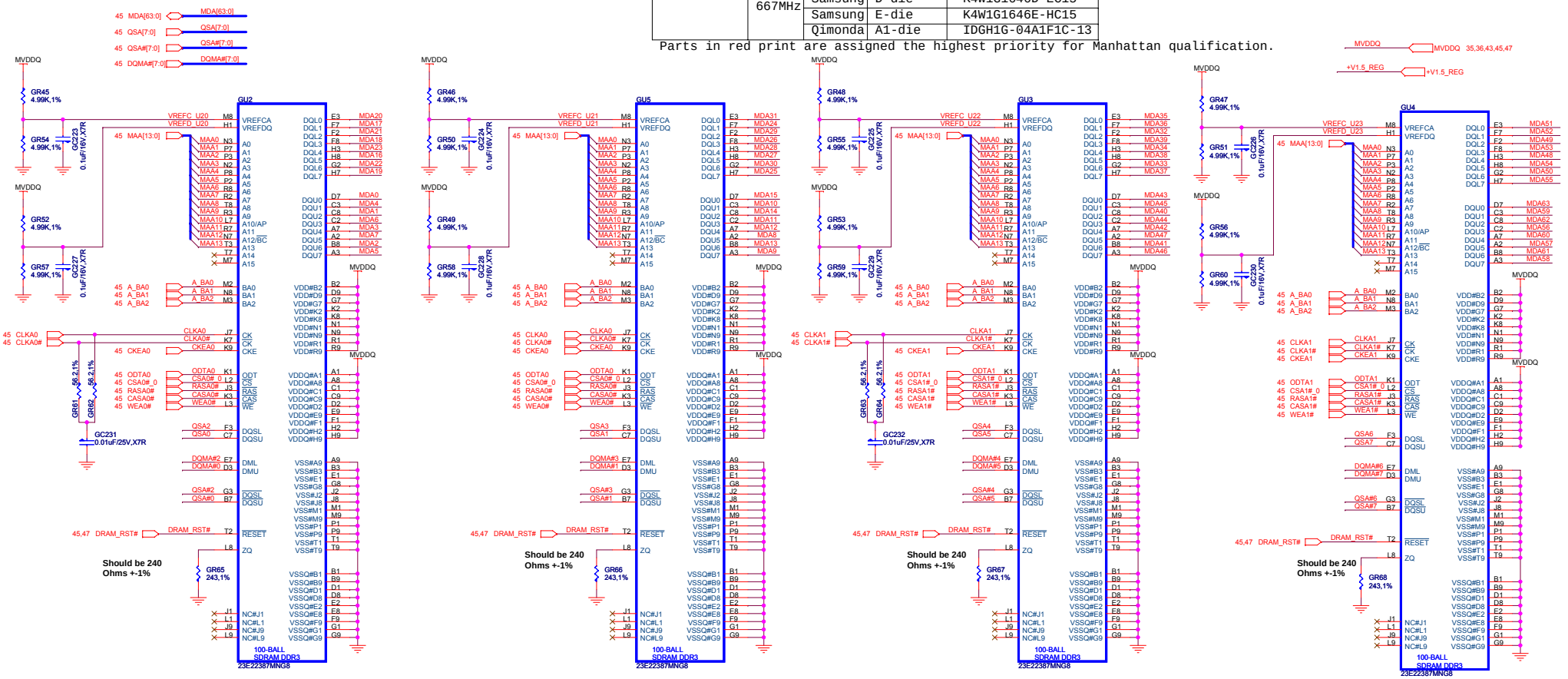
Date: Thursday, April 22, 2010 | Sheet 45 of 56

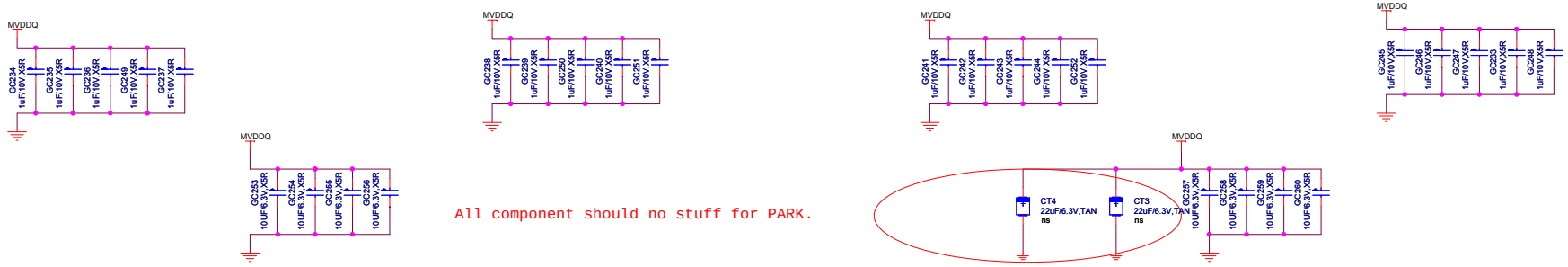
CHANNEL A: 256MB/512MB DDR3

Size per Part	Configuration	Row x Col x Bank bits
1024 Mbit	8 M x 16 x 8	13 x 10 x 3

DDR3 64M X 16bit	1GHz	Samsung	E-die	K4W1G1646E-HC1A
	900MHz	Qimonda	A1-die	IDGH1G-04A1F1C-18
		Samsung	E-die	K4W1G1646E-HC11
	800MHz	Hynix	Orion-die	H5TQ1G63BFR-12C
		Qimonda	A1-die	IDGH1G-04A1F1C-16
		Samsung	E-die	K4W1G1646E-HC12
	700MHz	Hynix	Tiva-die	H5TQ1G63AFR-14C
		Hynix	Orion-die	H5TS1G63BFR-1
	667MHz	Samsung	D-die	K4W1G1646D-EC15
		Samsung	E-die	K4W1G1646E-HC15
		Qimonda	A1-die	IDGH1G-04A1F1C-13

Parts in red print are assigned the highest priority for Manhattan qualification.



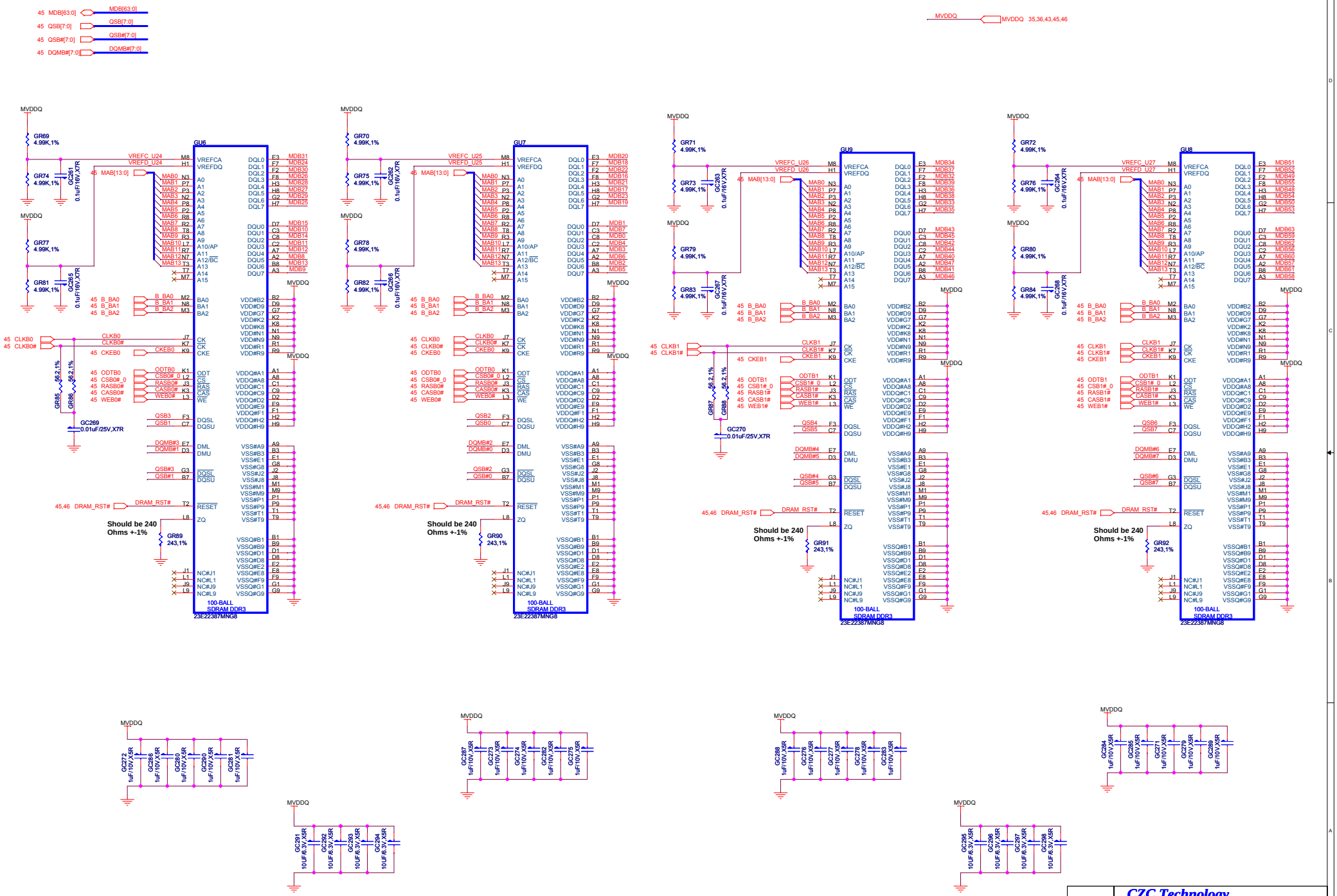


All component should no stuff for PARK.

CZC Technology

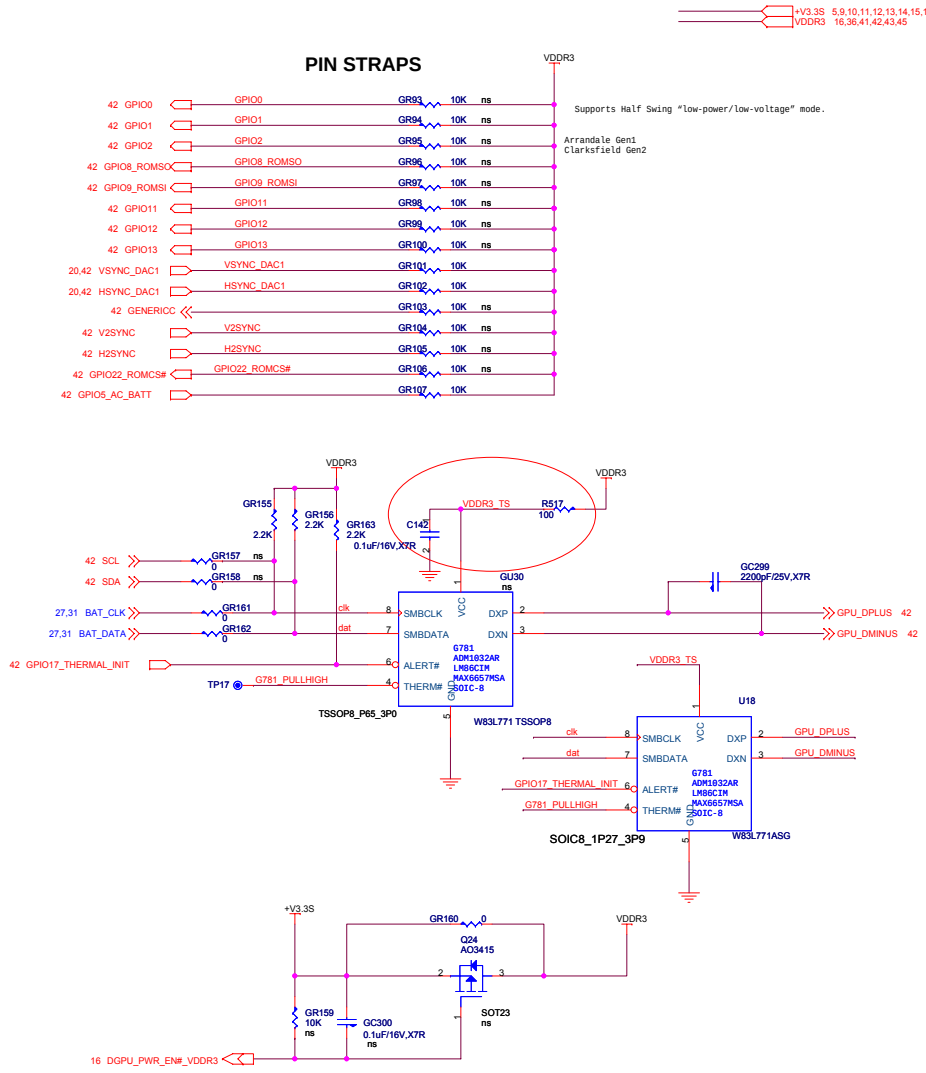
Title: Madison Memory DDR3 Channel A		zw
Size: C	Project Name: R48	Rev: C
Date: Thursday, April 22, 2010	Sheet 46 of 56	

CHANNEL B: 256MB/512MB DDR3



CZC Technology

Title	Madison Memory DDR3 Channel A	zw
Size C	Project Name R48	Rev C
Date: Thursday, April 22, 2010	Sheet 47 of 56	



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA DIS	GPIO9_ROMSI	VGA ENABLED	0
BIF_RX_PLL_CALIB_BP	GPIO21	BIF_RX_PLL_CALIB_BP	0
BIOS_ROM_EN	GPIO22_ROMCS#	ENABLE EXTERNAL BIOS ROM	1
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
SMS_EN_HARD	H2SYNC		0
CCBYPASS	GENERICC		0
AUD[1]	HSYNC_DAC1	built-in HDMI connector	1
AUD[0]	VSYNC_DAC1	Audio functiuon present	1

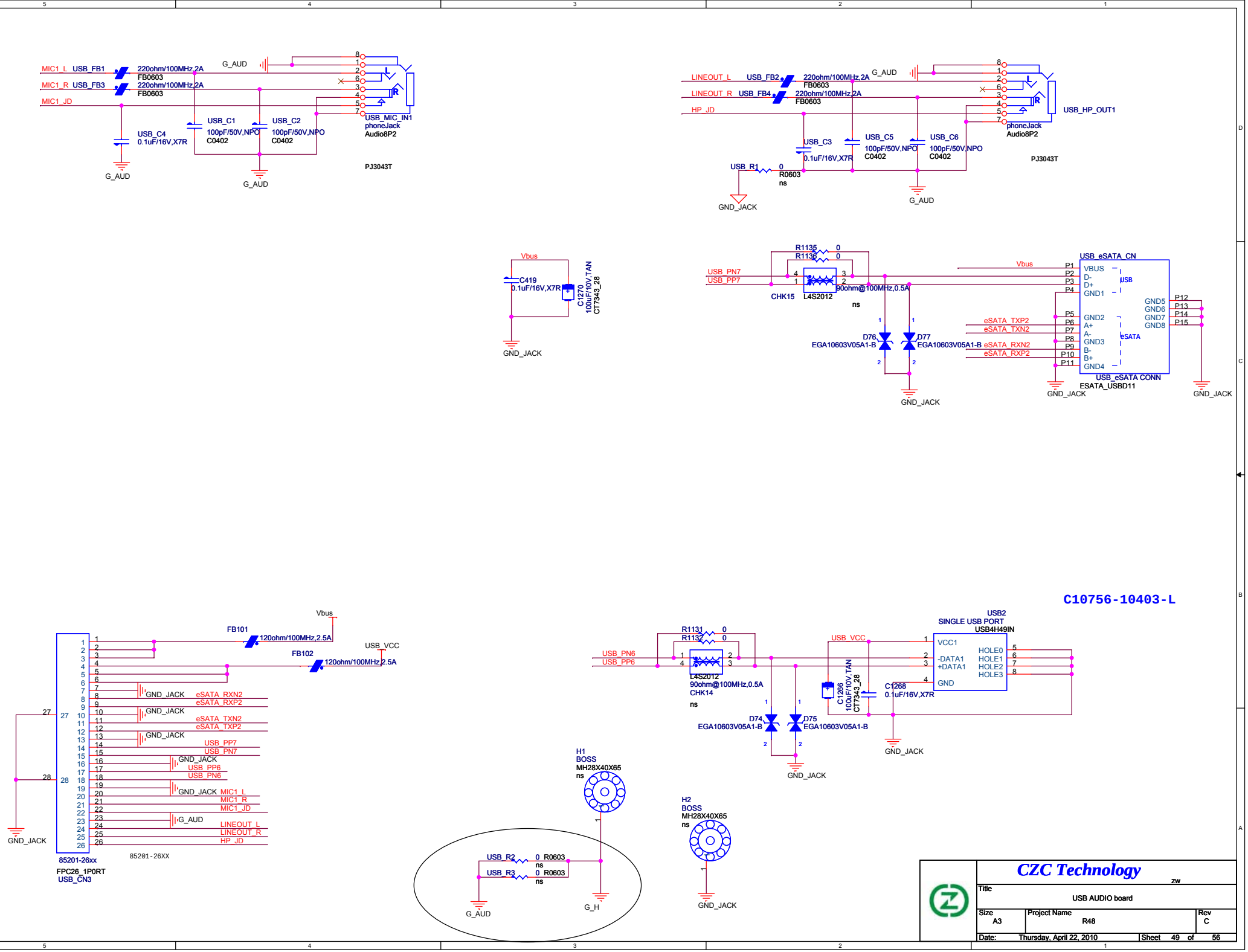
AMD RESERVED CONFIGURATION STRAPS

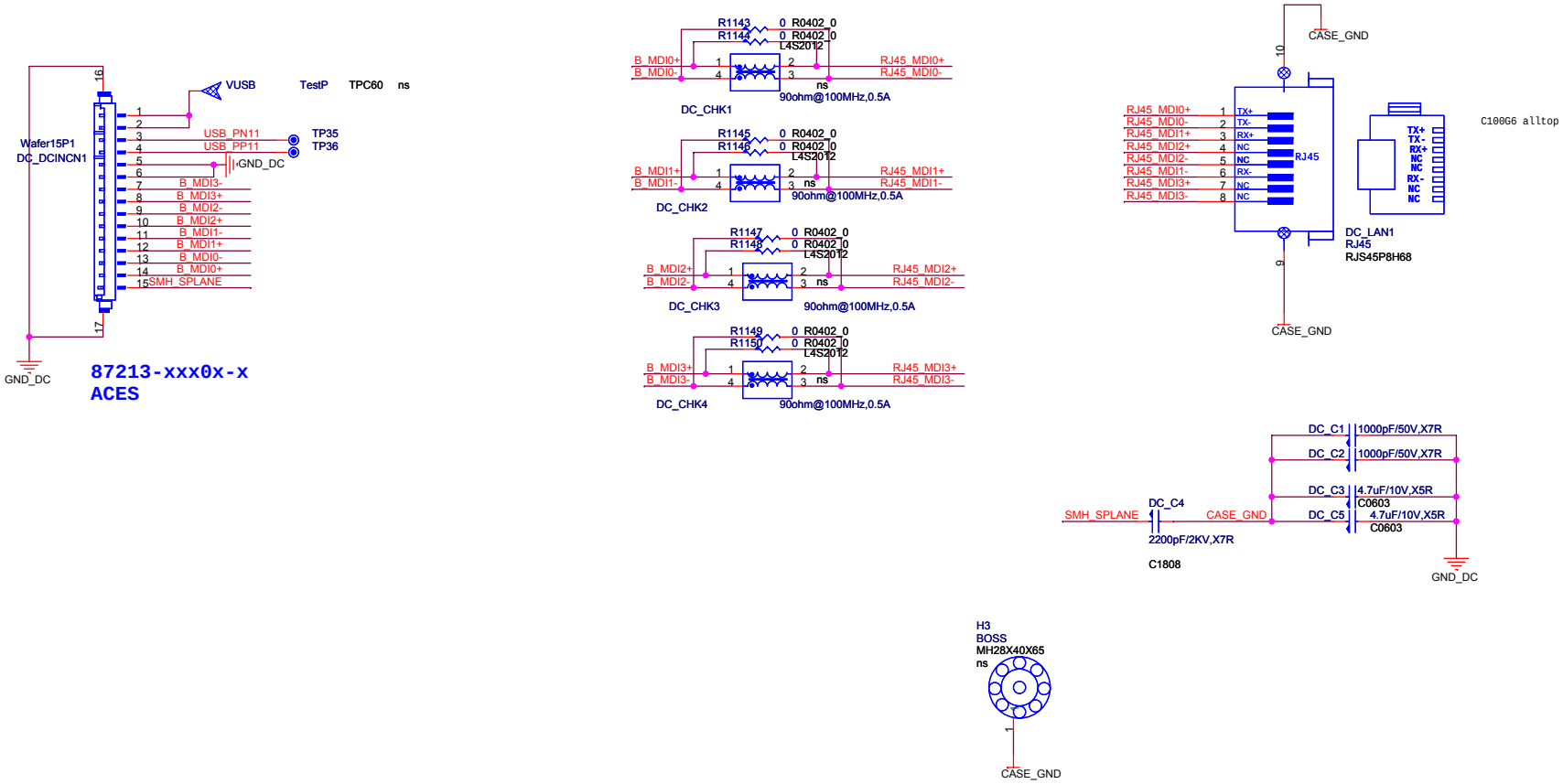
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

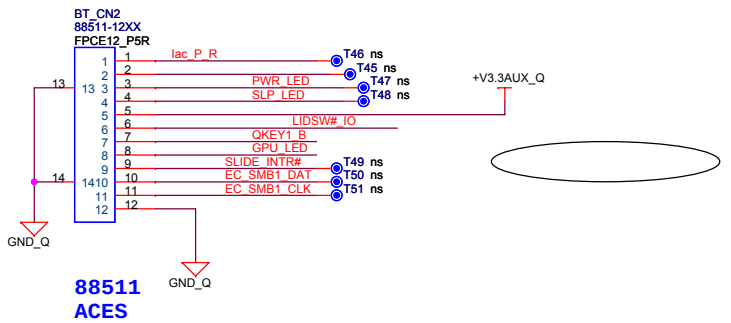
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

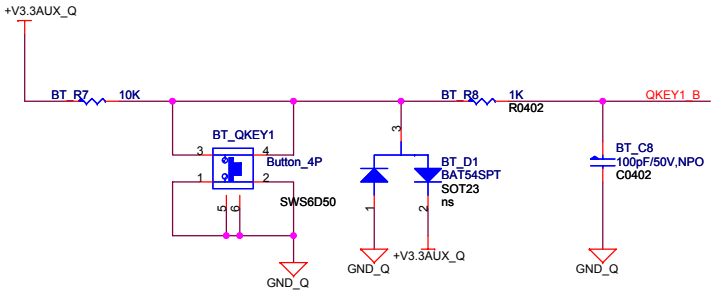
GPIO_28_TDO GPIO21_BB_EN

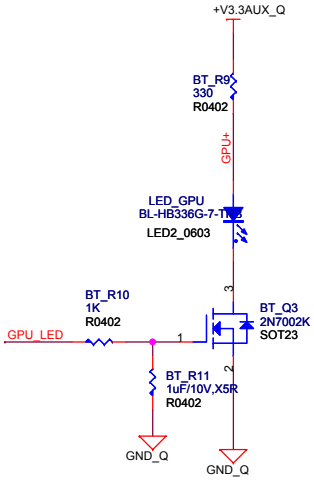

MIC1_L USB_FB1 220ohm/100MHz,2A FB0603
MIC1_R USB_FB3 220ohm/100MHz,2A FB0603
MIC1_JD
G_AUD
USB_C4 0.1uF/16V,X7R
USB_C1 100pF/50V,NPO C0402
USB_C2 100pF/50V,NPO C0402
USB_MIC_IN1 phoneJack Audio8P2
PJ3043T
LINEOUT_L USB_FB2 220ohm/100MHz,2A FB0603
LINEOUT_R USB_FB4 220ohm/100MHz,2A FB0603
HP_JD
USB_C3 0.1uF/16V,X7R
USB_C5 100pF/50V,NPO C0402
USB_C6 100pF/50V,NPO C0402
USB_R1 0 R0603 ns
GND_JACK
USB_HP_OUT1
Vbus
C419 0.1uF/16V,X7R
C1270 100uF/10V,TAN CT7343_28
R1135 0
R1136 0
USB_PN7
USB_PP7
CHK15 L4S2012 90ohm@100MHz,0.5A ns
D76 EGA10603V05A1-B
D77 EGA10603V05A1-B
eSATA_TXP2
eSATA_TXN2
eSATA_RXN2
eSATA_RXP2
USB_eSATA_CN
VBUS
D-
D+
GND1
GND2
A+
A-
GND3
B-
B+
GND4
GND5
GND6
GND7
GND8
USB
eSATA
USB_eSATA CONN
ESATA_USBD11
C10756-10403-L
FB101 120ohm/100MHz,2.5A
FB102 120ohm/100MHz,2.5A
USB_VCC
GND_JACK
eSATA_RXN2
eSATA_RXP2
eSATA_TXN2
eSATA_TXP2
USB_PP7
USB_PN7
USB_PP6
USB_PN6
MIC1_L
MIC1_R
MIC1_JD
LINEOUT_L
LINEOUT_R
HP_JD
85201-26xx
FPC26_1P0RT
USB_CN3
85201-26XX
R1131 0
R1132 0
L4S2012 90ohm@100MHz,0.5A CHK14 ns
C1266 100uF/10V,TAN CT7343_28
C1268 0.1uF/16V,X7R
D74 EGA10603V05A1-B
D75 EGA10603V05A1-B
USB2
SINGLE USB PORT
USB4H49IN
VCC1
-DATA1
+DATA1
GND
HOLE0
HOLE1
HOLE2
HOLE3
H1 BOSS MH28X40X65 ns
H2 BOSS MH28X40X65 ns
USB_R2 0 R0603 ns
USB_R3 0 R0603 ns
G_H
CZC Technology
zw
Title
USB AUDIO board
Size A3
Project Name R48
Rev C
Date: Thursday, April 22, 2010
Sheet 49 of 56

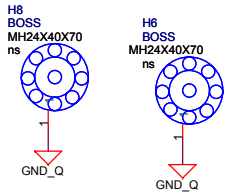


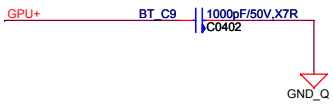
CZC Technology			
Title	RJ45		
Size A3	Project Name R48		Rev C
Date: Thursday, April 22, 2010	Sheet 50 of 56		

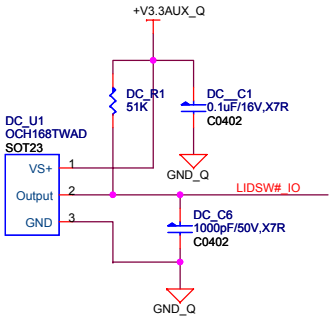








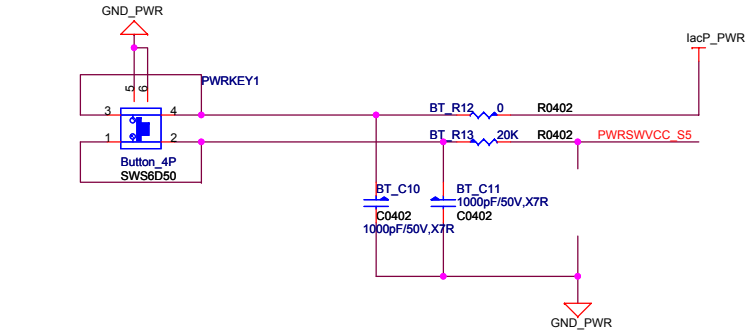


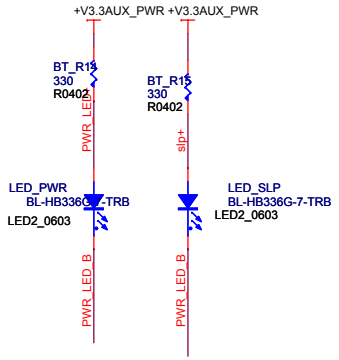


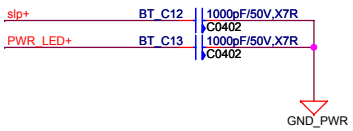
CZC Technology

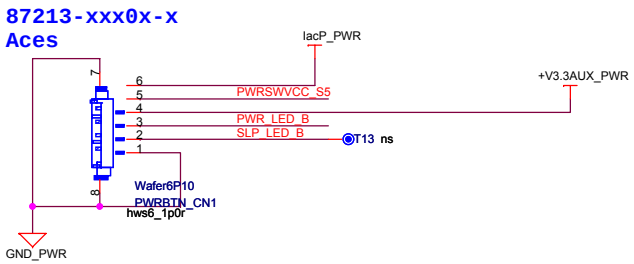
zw

Title	QKey LID Board	
Size A3	Project Name R48	Rev C
Date: Thursday, April 22, 2010	Sheet 51 of 56	





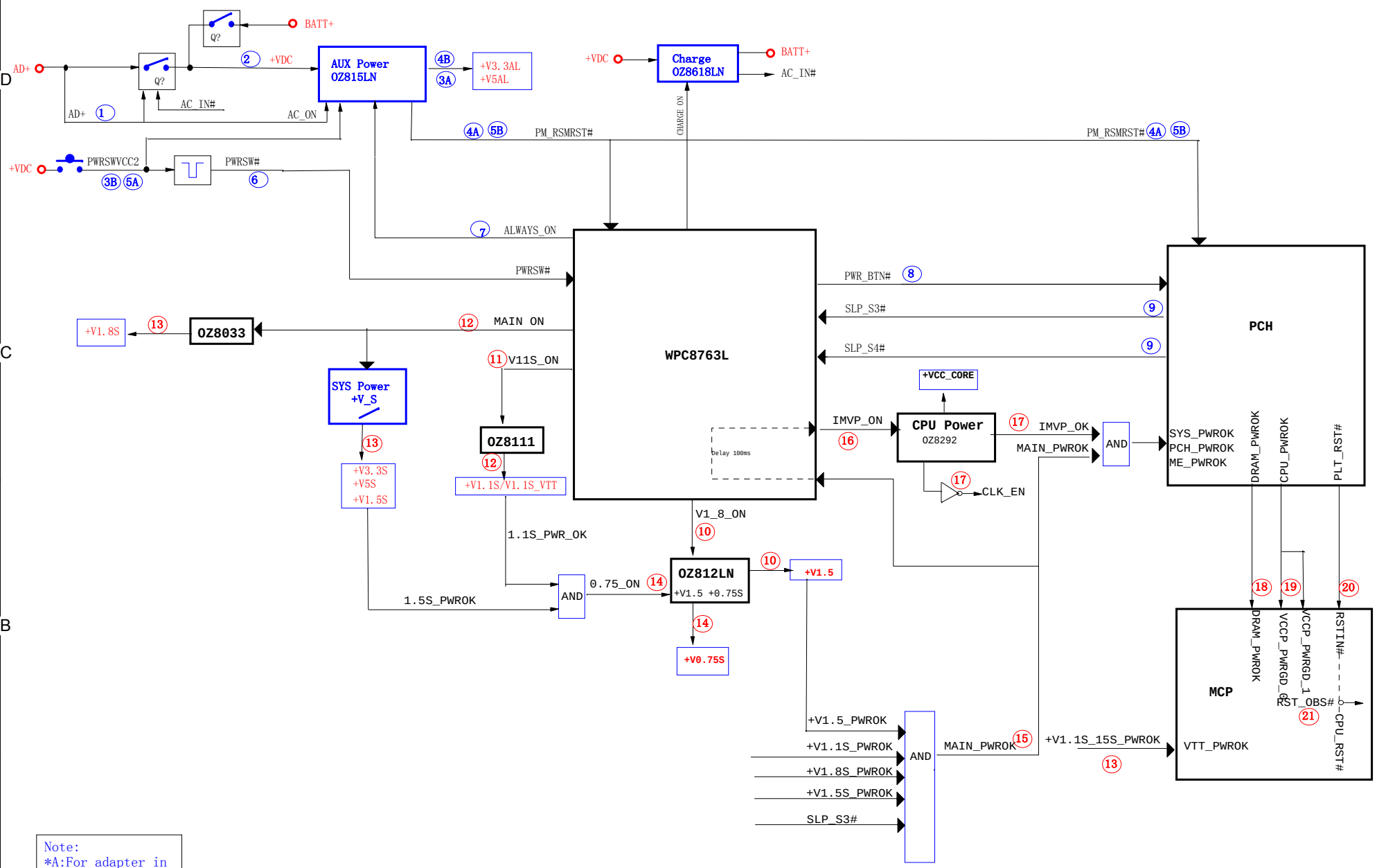




CZC Technology

zw

Title	PWR_BTN Board	
Size A3	Project Name R48	Rev C
Date: Thursday, April 22, 2010	Sheet 52 of 56	



Note:
*A:For adapter in
*B:For battery only
* :For all

CZC Technology			
Title: <Title>			
Size: A4	Project Name: R48		Rev: C
Date: Thursday, April 22, 2010		Sheet 53 of 56	

4. Schematic modify Item and history;

2009-12-03:
1. first Release and generate netfile.

2010-01-08:
1. P13 stuff R97。
2. P14 Add R359 R360
3. P16 Change R1005 pull high to VDDR3.
   No stuff R204
4. P19 Change D62 to R299
   Correct channel A/B connection of GPU LVDS.
5. P21 ns R457 R458
6. P22 Change NEW_CARD_CLKREQ# pull high to +V3.3S(R282)
7. P25 Add MDCCN1
   ns D26
7. P27 Add R436 1K,
   Add BT_LED# to EC
8. P29 change wifi LED connection,Touchpad CONN connection.
9. P42 Add GR125 GR126 GR127 for the Ver A11 of PARK. U27.1 change to Madison_pwrok.
10. P43 Add CT5 CT6 reserved.
11. P44 Add Q34 Q35 GR164 GC301
12. P45 Add GR165 for the Ver A11 of PARK.
13. P46 Add CT3 CT4 reserved.
14. P30-P40 change refer to SCH.

VerC change list:
hw:
1, 修改部分0ohm电阻封装为R0402_0
2,ns thermal sensor for DIMM(P09)
3,ADD BIOS_LOCK SWITCH。(P13)
4, ns MiniPCIE slot for 3G.(P21)
5,ns C1280 C1230 C1234(P24)
6,Reserved TPA6017A2,adjust amp out(p25)
7,add R524,change R449 to 200K,for fan(p28)
8,ns U19,stuff R1152(p41)
9,add R517 (P48)
10,del BT_Z1 (P52)

pwr:
1、更改R917 R919阻值，设定DDR3电源1.54V
2、1.1S电源增加R1187 R1186 C1296频率调整电路
3、更改R939 R937阻值，调整1.1S电源为1.129V
4、去掉电阻R1179 0ohm电阻，去掉D69续流二极管，更改R978 1K 5%为1K 1%，
5、R1153，R1154，C1277更改value设定GFX电源频率在350KHz
6、OZ8291 DSLP pin改成2.2Kohm下拉到地
7、R1181阻值更改以满足IMONITOR
8、去掉OZ8291 VID 测试电路
9、更改R1014阻值以满足cpucore的loadline，更改R1016 1K 5%为1K 1%，去掉R1182 0ohm电阻
10、OZ8292 DSLP pin接2.2K电阻上拉到5VS以满足imvp6.5
11、更改R1184阻值以满足IMONITOR,去掉D70 D71续流二极管，去掉OZ8292 VID 测试电路

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